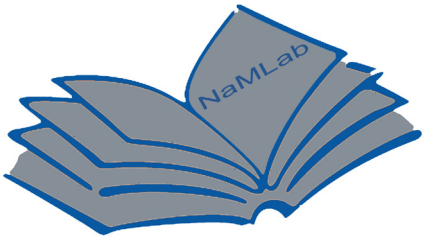
Two-Year Report 2022.2023

Highlights 2022/2023

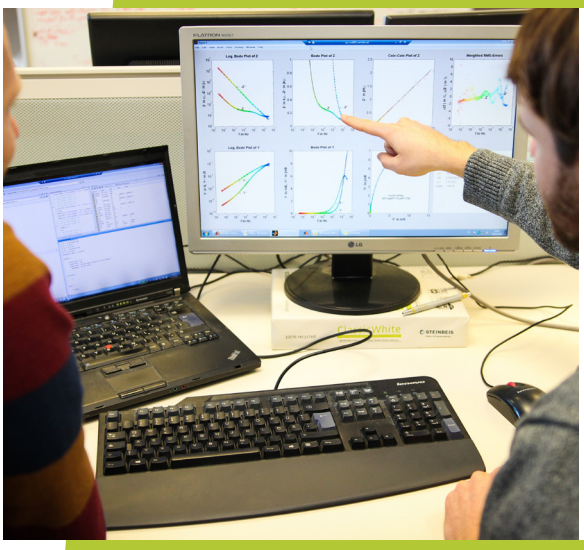
Employees	PhD Students
41	17



Publications	Citations
106	>11000

Patent applications/ Patents	Research Projects
5/2	28

Content



Prof. Dr.-Ing. Thomas Mikolajick

Preface

NaMLab was founded in 2006 as a public private partnership between Qimonda Dresden GmbH and TU Dresden. In the first year, NaMLab started as a research organization with 10 employees focused on material research for future memory devices. The company steadily expanded and today, NaMLab serves a growing list of world-wide partners. NaMLab´s research is contributing to the main challenges for our future society with respect to climate change, digitalization and mobility by placing sustainable, secure and intelligent electronic solutions into the core focus. With respect to the technical areas those solutions can be divided into three main activities:

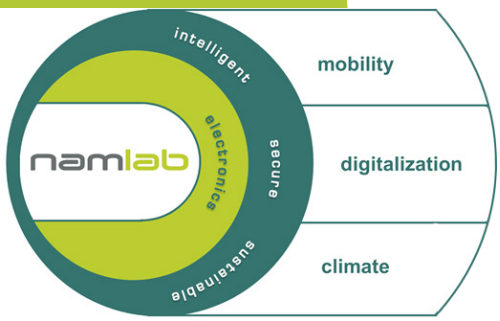
- Dielectrics for Semiconductor Devices,
- Reconfigurable Devices and
- Energy Efficiency Devices

This seventh bi-annual report covers the NaMLab activities in the two-year period 2022 and 2023. The timeframe was influenced by the Attack of Russia on Ukraine. Especially the rising and not predictable costs for electrical power, district heat, and materials like liquid Nitrogen in conjunction with the overall high inflation rate have been a strong burden for a research organization having a cleanroom and working on semiconductor technology. Once again, the team met the challenge with great success. Programs to reduce power consumption and consumables were put in place. By this the institute could continue its path as a world leading organization in the field of material research for future electron devices. The level of international attention has further increased as visible by invitations to world leading conferences.

NaMLab´s research in the field of dielectrics is focused on novel and semiconductor compatible ferroelectric materials, such as hafnium oxide and aluminum scandium nitride, and their application in capacitors. Understanding the most important factors that control ferroelectricity, as well as understanding the degradation mechanism of such ferroelectric materials was a focus of the research in the reporting period. As an example of a highlight, the advanced material stacks were successfully integrated into a 1T-1C FeRAM demonstrator using a 3D capacitor . This shows the strong relation between materials research on dielectrics and the device oriented topics NaMLab has achieved.

All three reconfigurable device concepts explored at NaMLab are currently under consideration for applications in both intelligent self-learning electronics as well as electronics with a higher inherent security.

In a reconfigurable field effect transistor (RFET), the polarity of a field effect device can be controlled by applying a gate voltage to a dedicated programming gate. In the reporting period, the team, together with an industrial partner, was able to demonstrate a first RFET device integrated into a state of the art CMOS technology. It was shown that a reconfigurable analog function is possible with only minor modifications of the standard CMOS integration process. Moreover, the path towards applications in hardware security was further extended.



The research activities of NaMLab are connected to the main societal challenges: mobility, digitalization and climate change by focusing on intelligent, secure and sustainable electronic devices.

Dielectric materials

Capacitor Dielectrics
Fluorite Structure Ferroelectrics

Reconfigurable Devices

Nanowire Devices
Ferroelectric Devices
Resistive Switching Devices

Energy Efficiency Devices

GaN devices

Overview of research activities at NaMLab

The second topic in reconfigurable devices is field effect transistors based on ferroelectric hafnium oxide. Together with partners from Fraunhofer IPMS-CNT and GlobalFoundries, NaMLab is pushing this concept since 2009.
On this topic in the reporting period, NaMLab continued by working with GlobalFoundries and the NaMLab Spin-Off Ferroelectric Memory GmbH on developing the embedded FeFET technology at GlobalFoundries. Applications of ferroelectric hafnium oxide beyond semiconductor memories like neuromorphic computing and memory-in logic devices were a focus point. Moreover, the work on ferroelectric tunneling junctions (FTJ) to realize artificial synapses have become more important with new EU projects coming on-line.
The third major reconfigurable device concept explored is resistive switching. Here, analog resistive switching as well as memcapacitance was pushed further and together with partners of TU Dresden a new concept of a neurotransistor was proposed and a project to realize it experimentally was started.
The field of energy efficiency devices had three key topics, namely solar cells, batteries and GaN materials and devices in the past. All three research activities aim on providing sustainable electronic solutions. The solar cell and battery activities were not continued in the reporting period. For solar cells this was caused by the overall situation of solar industry in Germany. In the field of batteries the focus of research has shifted away from nanowire-based anodes, which have been the main focus of research at NaMLab
In the field of gallium nitride materials and devices at the outpost in Freiberg, together with its industrial partner NaMLab was able to further enhance the quality and reproducibility of crack-free doped HVPE GaN crystals and the scaling-up of wafer diameter was initiated. IIWith the MBE activities high quality films reflecting the understanding of the emergence and the impact of remaining impurities was further improved. These activities have been hit by the attack of Russia on Ukraine since the very fruitful collaboration with the Russian partner had to be stopped. As a new activity in the field of GaN devices, research combining NaMLabs know how on ferroelectrics with GaN transistor technology was started.
In summary, despite the complicated boundary conditions induced by the attack of Russia on Ukraine, NaMLab further strengthen its position in the core topics in the reporting period, contributing to the grand challenges of our modern society. This is documented in the increasing number of partnerships with local and international industrial and research partners. Another impressive increase of citations of NaMLab's scientific publications as well as a large number of invitations to leading scientific conferences like IRPS, ISAF, EDTM, IEDM, VLSI-TSA document the high international visibility NaMLab has now achieved and maintained. The NaMLab team will built on the strong results accomplished in this reporting period and further extend its efforts to continuously contribute to shape the exciting and challenging world of micro- and nanoelectronics.

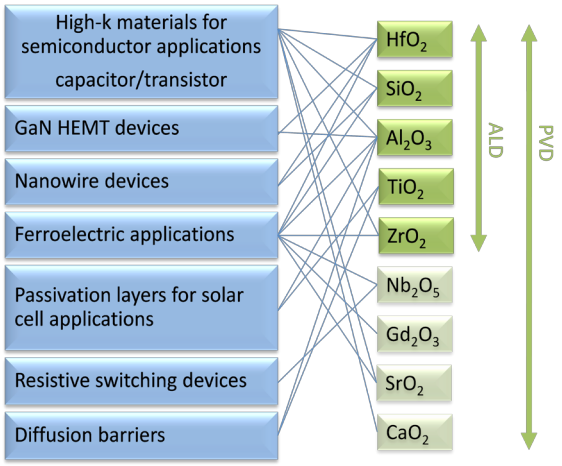
Prof. Dr.-Ing. Thomas Mikolajick

Dielectric Materials

Dielectrics

High-k materials play an increasingly important role in nanoelectronic devices; for example, conventional semiconductors store charge in capacitors with a dielectric insulating layer. To maintain the storage capacity of capacitors, new dielectric materials with higher dielectric constants need to be introduced for smaller area devices. Similar dielectric materials are required for the next generation of high-performance transistors for processors and logic products. Several research projects are underway at the nanoscale level to understand the properties of the materials in terms of leakage mechanisms, performance, speed, and reliability.

The schematic below shows five key material systems (Al_2O_3, HfO_2, ZrO_2, TiO_2, and SiO_2) that have been studied for various dielectric applications. Accordingly, a detailed understanding of the structural and electrical properties obtained for one device application can provide a fundamental knowledge base for future new devices. The effect of process conditions on device performance can be correlated. In particular, the optimization of material properties such as density, dielectric, piezoelectric, ferroelectric, and optical properties or charges and traps is essential for different device applications.



NaMLab also screens and characterizes other candidate materials for novel device applications. Examples include Nb_2O_5, La_2O_3, SrO_2, Sc_2O_3, and $CaTiO_3$, additional novel dielectrics will follow. Materials are deposited by Atomic Layer Deposition (ALD), Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD), and Molecular Beam Deposition (MBD), as shown in the drawing above. Research at NaMLab covers a wide range of applications, from dielectrics for nanowire transistors (Fig. 1), GaN HEMT devices (Fig. 2), to ferroelectric $HfZrO_4$ based capacitors (Fig. 3).

Contact: Dr. Uwe Schroeder

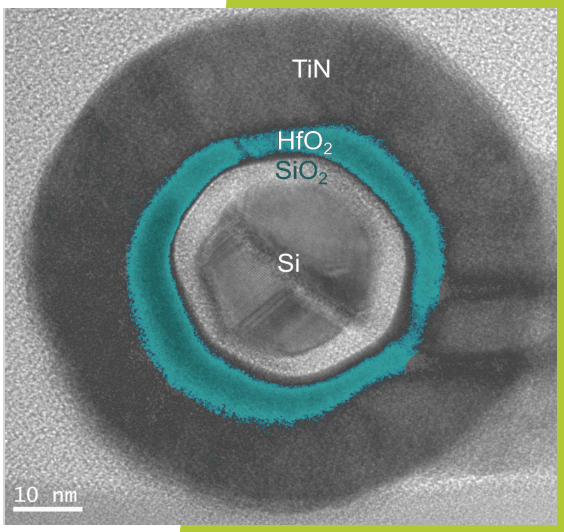


Fig. 1: ALD based dielectric materials as gate dielectric in nanowire and ferroelectric field effect transistors.

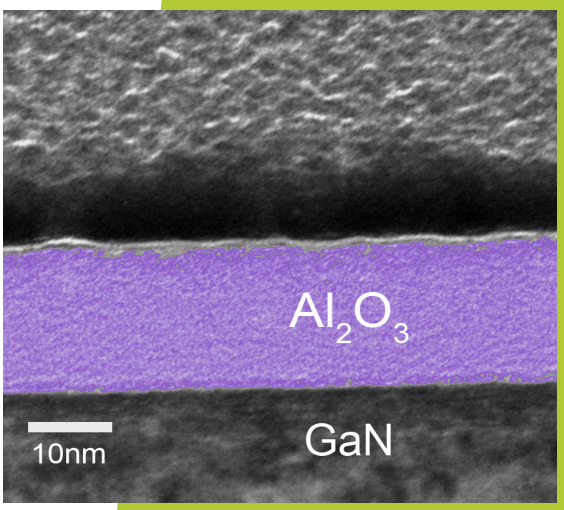


Fig. 2: Deposition of ALD Al_2O_3 dielectrics within a GaN HEMT device.

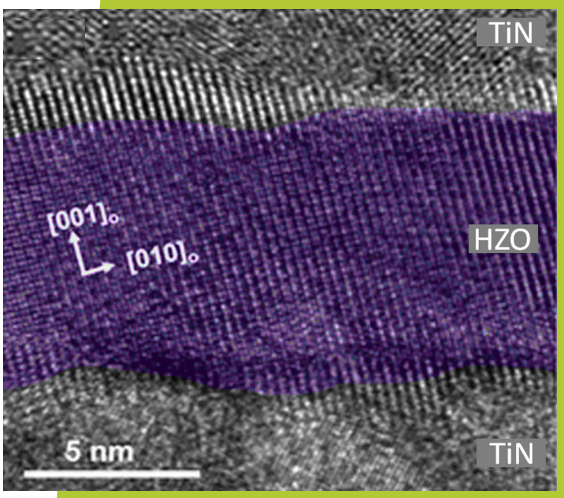


Fig.3: Deposition of ALD $HfZrO_4$ dielectric in a capacitor structure.

Hafnium Oxide Based Ferroelectric Materials

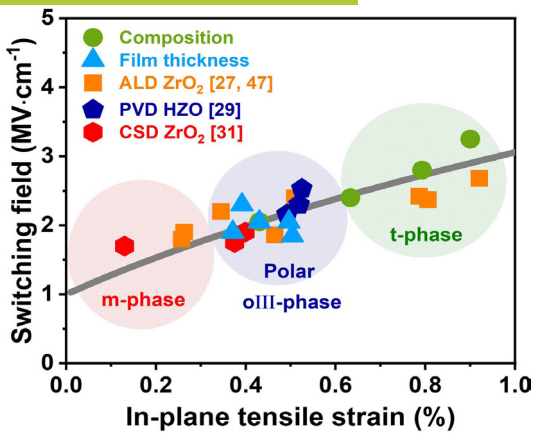


Fig. 1: Switching field (Ec for ferroelectric films and t- to o-phase transition field for anti-ferroelectric films) as a function of in-plane-tensile strain for films from different sources.

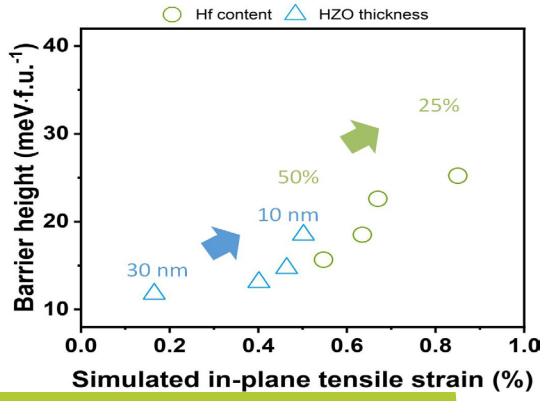


Fig. 2: Simulated barrier height as a function of in-plane tensile strain

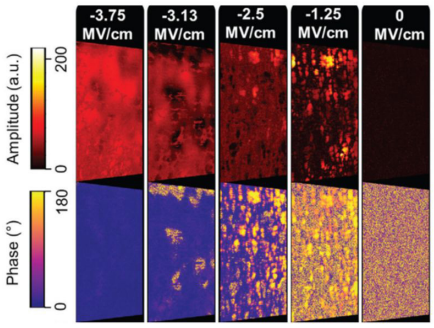


Fig. 3: BE-PFM images of 350 nm × 350 nm of ZrO_2 with DC electric field biases: snapshot evolution of the electric field-induced phase transition.

During the last two years, the main focus of developing ferroelectric HfO_2-based materials is the detailed understanding of the ferroelectric properties in thin doped HfO_2 layers. A variety of dopant materials were studied in addition to a mixed $Hf_{1-x}Zr_xO_2$. Deposition techniques included atomic layer deposition and physical vapor deposition. The ferroelectric orthorhombic $Pca2_1$ phase of HfO_2 is formed when the material is crystallized with a certain dopant or oxygen concentration at the phase boundary between the monoclinic and the tetragonal/cubic phase and is enhanced through mechanical confinement. Scanning transmission electron microscopy and electron diffraction methods confirmed the structure. Continuous research aims to understand the root cause of this previously unknown phase. Here, dopant and oxygen content, which are directly related to stress and strain in the layer, play an essential role in phase stabilization. A linear relation between strain and the coercive field of the phase transition field was found (Figure 1). These parameters impact thermal stability and film reliability. Based on these results, significant improvements in the film performance could be achieved. Ab initio simulations by partners at the Munich UAS confirmed the influence of the factors mentioned above on the phase stability of ferroelectric HfO_2 and proposed a similar relationship of barrier height for ferroelectric switching as a function of strain (Figure 2).

Depending on the dopant material, the polarization hysteresis showed a maximum remanent polarization value between 15-40 µC/cm². The highest values were obtained for lanthanum-doped HfO_2 with TiN electrodes. Piezo-response force microscopy (Oak Ridge Nat. Laboratory/Univ. Nebraska), in conjunction with transmission electron microscopy measurements, revealed domains within single grains with a diameter of ~20-30 nm for 10 nm thick films. For ZrO_2, a field-induced transition from non-polar to polar grains is found, as expected for a tetragonal to orthorhombic phase transition (Figure 3). The polycrystalline structure of the films caused a varying polarization orientation within the layer. The size distribution of the grains follows a Poisson distribution, resulting in a grain size-dependent coercive field and Curie temperature.

Future studies will focus on the structural basis of the ferroelectric properties, their impact on the ferroelectric switching behavior, and how device cycling performance can be improved.

Cooperation: Fraunhofer IPMS-CNT, Dresden (Germany), RWTH Aachen (Germany), UAS Munich (Germany), GLOBALFOUNDRIES Dresden (Germany), IMEC (Belgium), Oak Ridge National Labs (USA), University of Nebraska (USA), Tokyo Institute of Technology (Japan), TU Eindhoven (Netherlands), University of Helsinki (Finland)

Publications: J2, J3; J5, J12, J14, J16, J17, J18, J26, J27, J28, J35, J37, J48, J50, J52, J56, J57, J58, J59, J60, J67, C12, I1, I3, I6, I9, I11, I12, I13, P3

Contact: Dr. Uwe Schroeder

Hafnium Oxide Based Pyro-electric Materials

The main focus of the work is on a detailed understanding of the pyroelectric properties (PE) in thin doped HfO_2 layers. Pyroelectric properties were characterized for various doped HfO_2 and $Hf_{1-x}Zr_xO_2$ films with different thicknesses.

A survey of the pyroelectric behavior was undertaken for a wide variety of dopants incorporated into HfO_2 including Al, Gd, Sr, and La as well as the $Hf_{0.5}Zr_{0.5}O_2$ composition. In addition to understanding the effect of different dopants, a detailed investigation of the pyroelectric dependence on the Si-concentration in Si-doped HfO_2 thin films was carried out to evaluate the influence of the doping concentration on the pyroelectric performance. The Sharp-Garn method detects the current response upon a sinusoidal temperature stimulation was used to accurately determine the pyroelectric coefficients in ferroelectric films. Infrared sensing applications for example require a linear and reversible transduction of temperature into electrical charge (Fig. 1).

A new pyroelectric device was developed that incorporated antiferroelectric Hf-doped ZrO_2 within a work function (WF) engineered capacitor, where electrode materials of TiN and RuO_x were used to generate a constant internal electric field. This innovative development not only produces a zero applied field (passive) pyroelectric response from antiferroelectric thin films, but it also enables non-volatile on/off switching of the pyroelectric effect via bipolar voltage pulses.

To distinguish and quantify the pyroelectric properties of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ and WF-engineered ZrO_2 thin film capacitors, both the poling and film thickness dependence was investigated. The pyroelectric coefficient in $Hf_{0.5}Zr_{0.5}O_2$ was found to exhibit an electric field poling dependence due to the different polarized states of the ferroelectric films, whereas in the WF-engineered antiferroelectric ZrO_2 capacitor the pyroelectric coefficient can be set either to -90 or 0 $\mu C\ K^{-1}\ m^{-2}$ depending on the polarity of the poling field (Fig. 2). With strong pulsed poling fields, the pyroelectric coefficient saturates by maximizing the remanent polarization induced in the ferroelectric films. The role of film thickness was determined by varying $Hf_{0.5}Zr_{0.5}O_2$ films from 10 – 30 nm in thickness. The highest pyroelectric coefficients and best figures of merit were obtained in 10 – 15 nm $Hf_{0.5}Zr_{0.5}O_2$ thin films annealed at 450 °C (Fig. 3), whereas the pyroelectric performance in thicker films and higher annealing temperatures was degraded due to the formation of the monoclinic phase and low-k interfacial layers. Through the Landau-Devonshire Gibbs energy equation for ferroelectrics, a relationship between the dielectric, ferroelectric, and pyroelectric properties was established in all types of HfO_2-based thin films by the Curie constant.

Cooperation: RWTH Aachen (Germany), Hochschule München (Germany), Oak Ridge National Labs (USA), TU Bergakademie Freiberg (Germany)

Publications: I10

Contact: Dr. Uwe Schroeder

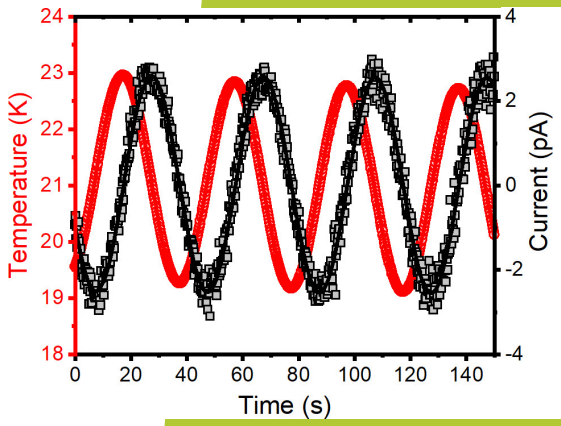


Fig.1: Sharp-Garn pyro-electric measurement performed on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$.

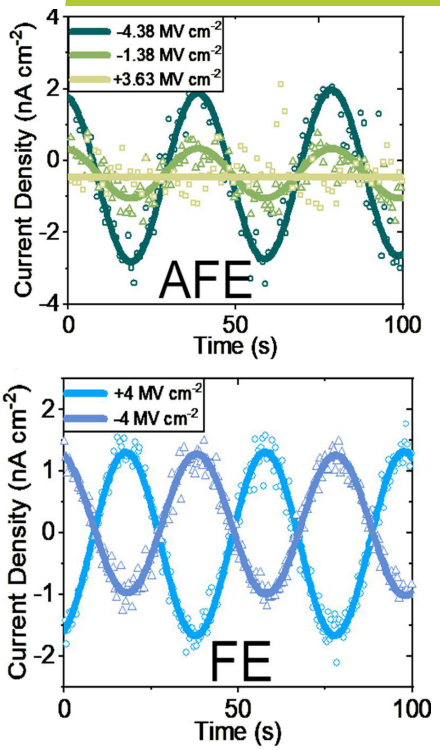


Fig.2: Poling field dependence of the pyroelectric coefficient in $Hf_{0.5}Zr_{0.5}O_2$ and WF engineered $Zr_{0.87}Hf_{0.13}O_2$ thin film capacitors.

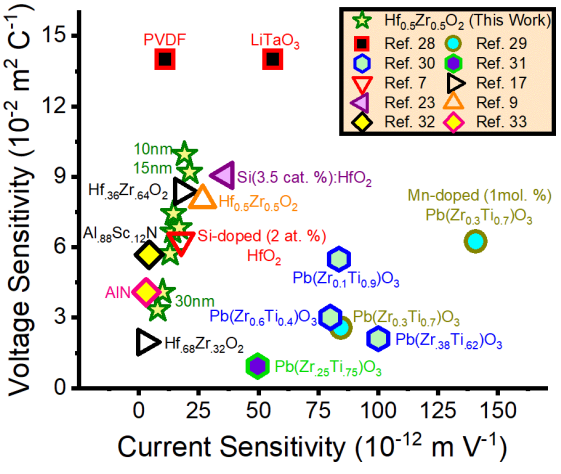
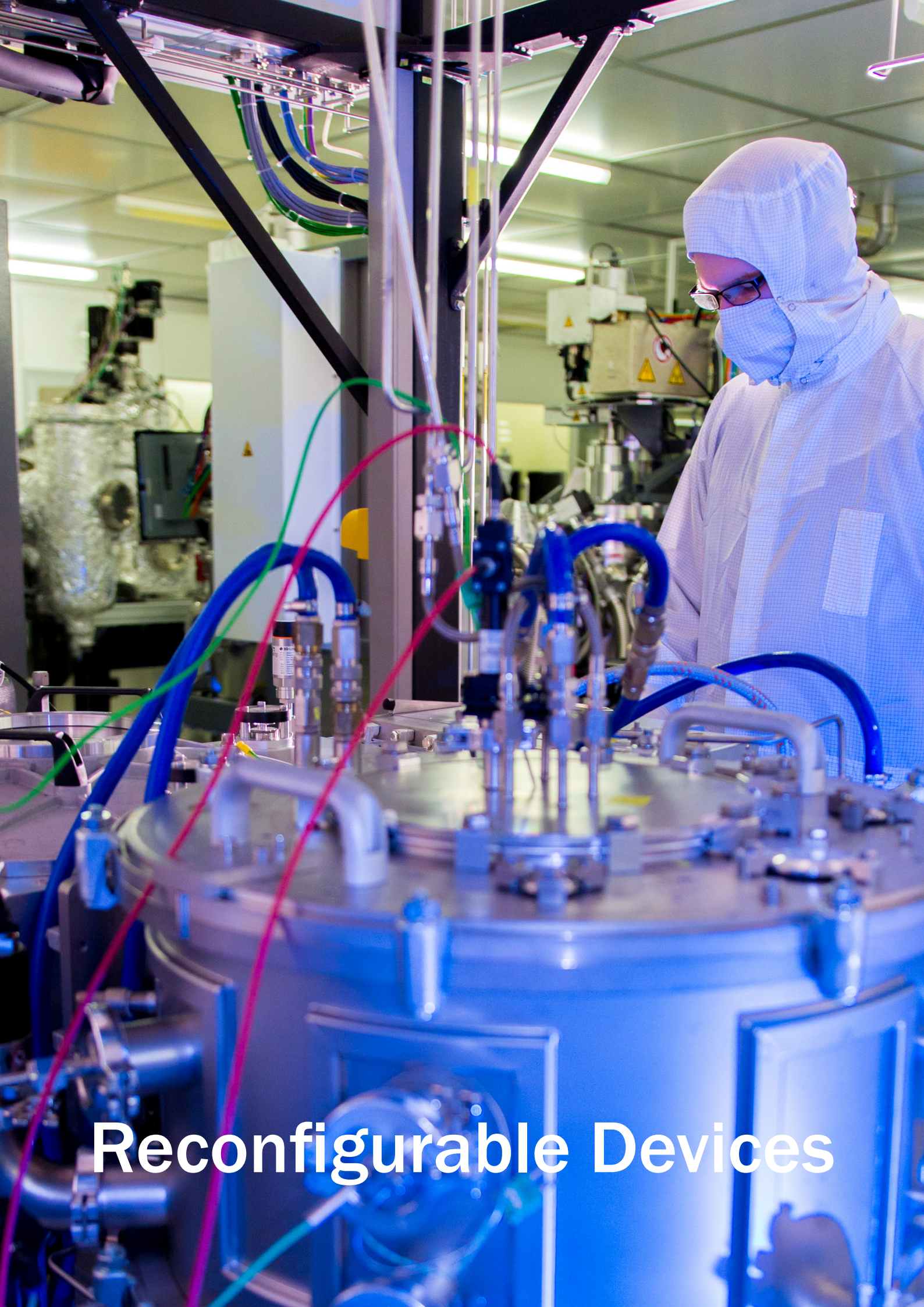


Fig. 3: Voltage sensitivity and current sensitivity figures of merit of $Hf_{0.5}Zr_{0.5}O_2$ thin films of different thicknesses for infrared sensor material benchmarking.



Reconfigurable Devices

Capacitor Based Ferroelectric Memory

During the last reporting period, the main focus was on transferring the metal-ferroelectric-metal capacitor stack from the lab, having a diameter of about 100 µm, to memory arrays with 100-1000 times smaller feature sizes. Concurrently, optimizing the film and film stack properties to improve the reliability of the ferroelectric capacitor according to industry specifications was addressed. The goal is to develop back-end-of-line compatible capacitors with a maximum thermal budget of 500 °C or below. The ferroelectric material of choice is an atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$. The activity was conducted with industrial partners, including LETI and ST, Sony, and Intel. 16, 64, and 1000 kbit-sized memory arrays with $Hf_{0.5}Zr_{0.5}O_2$-based capacitors were realized with a high yield on 200 mm hardware.

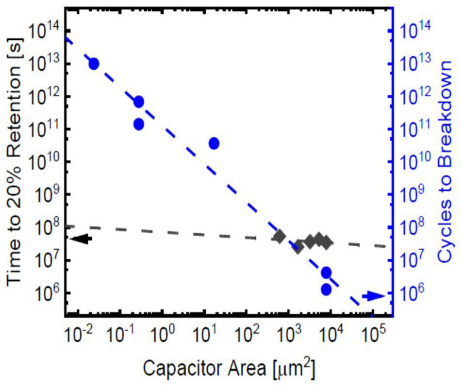


Fig. 1: Comparison of time to 20% retention and cycles to breakdown vs. capacitor area. (IEDM 2022).

The polarization hysteresis of $Hf_{0.5}Zr_{0.5}O_2$ -based capacitors showed a maximum remanent polarization of about 25 µC/cm². In addition, the influence of interface layers with $Hf_{0.5}Zr_{0.5}O_2$ on the field cycling behavior was examined, and stable cycling behavior of up to 10^{10} cycles was achieved. Scaling of the devices below 1 µm² improved cycling endurance. Values can be extrapolated beyond 10^{12} cycles for 2.5 MV/cm² target field conditions. (Figure 1) Wake-up, internal bias fields, fatigue, imprint, and retention effects in $Hf_{0.5}Zr_{0.5}O_2$ are generally dominated by charge trapping effects at defects mainly located at the $Hf_{0.5}Zr_{0.5}O_2$/electrode interface. Furthermore, depolarization effects can be caused by nonpolar phases. The duration of the ALD oxidant pulse strongly impacted the ferroelectric properties and device reliability, which was then used to optimize ALD processing. Due to the resulting voltage-time trade-off to achieve > 90% domain switching after 20 ns, a 2.5 MV/cm² field must be applied to layers with below 10 nm thick films.

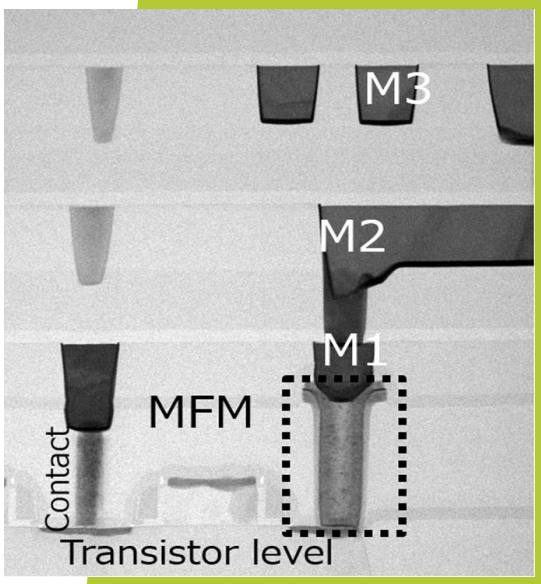


Fig. 2: SEM cross-section of Hf0.5Zr0.502 films within a 1 Mbit 3D capacitor-based memory array fabricated by partner Sony (IEDM 2023).

Development partners introduced the $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric material into their memory arrays and reached a field cycling endurance > 10^{11} for sub-1 µm 3D capacitor structures (Figure 2). Sense amplifiers read out stored polarization states and have a good read voltage margin with a 2.5 V operation voltage. They confirmed an operating speed of about 20 ns for 16 to 1000 kbit memory arrays (Figure 3).

Future studies will focus on further understanding the structural basis of the ferroelectric properties and their impact on the ferroelectric switching behavior to improve cycling performance for introduction into larger memory arrays.

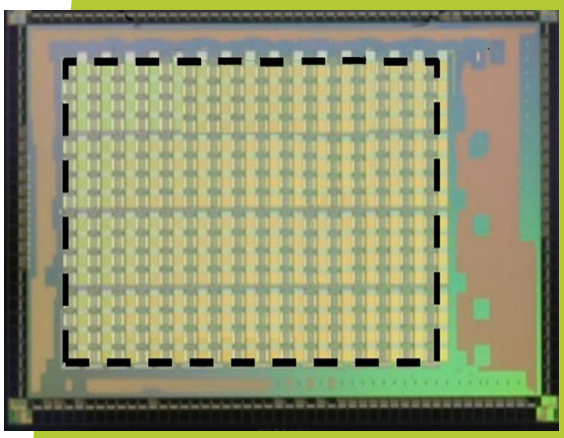


Fig. 3: Optical microscope image of 1 Mbit (dotted line) capacitor-based memory array fabricated by partner Sony (IEDM 2023).

Cooperation: CEA Saclay / CEA-LETI (France), ST Microelectronics (France), National Institute of Materials Physics (Romania), EPFL (Switzerland), Ecole Centrale De Lyon (France), NCSR „DEMOKRITOS“ (Greece), Intel, Forschungszentrum Jülich (Germany), Sony (Japan)

Publications: J5, J36, J41, J42, J51, C3, C18, C27, C28, I1, I3, I4, I5, I6, I8, I11

Contact: Dr. Uwe Schroeder

Ferroelectrics for beyond von Neumann computing

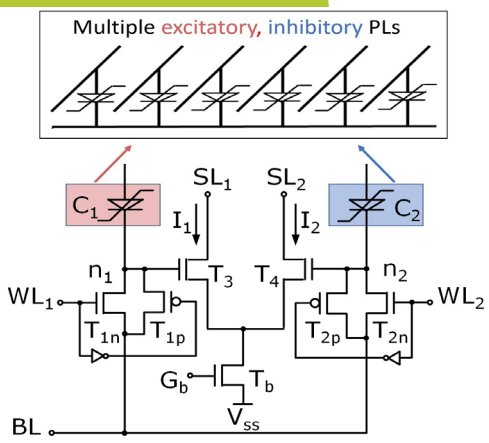


Fig. 1: A differential synaptic cell based on a 2T1C architecture can be expanded to integrate many capacitors on a single branch. This allows a parallel readout which greatly reduces read energy, and opens up possibilities for hyper dimensional computing and logic applications using FTJs or ferroelectric capacitors.

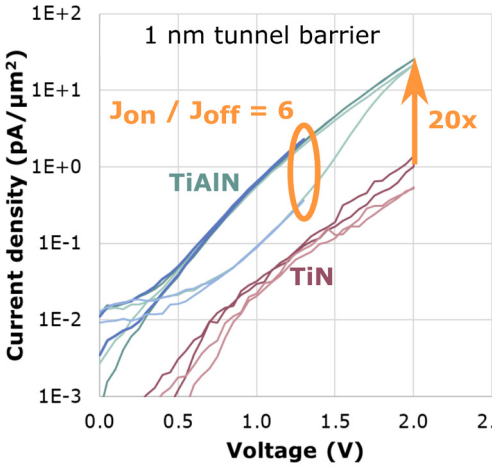


Fig. 2: The tunnelling current densities of bilayer HZO/Al2O3 can be increased significantly via work function engineering of the electrodes (reducing WF with TiAlN) and reducing tunnel barrier thickness to 1 nm. This leads to 100x improvement compared to the original devices.

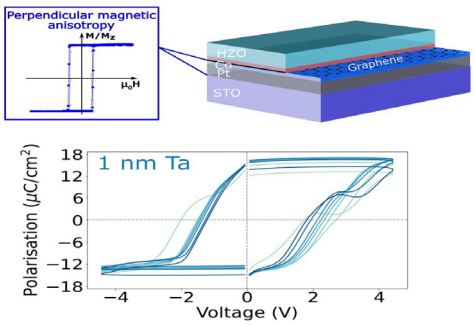


Fig. 3: Ferroelectric hafnia was integrated on graphene using an oxidized Ta interlayer. The thickness of the interlayer could be optimized to increase 2Pr up to 28 µC/cm² without decreasing the magnetic anisotropy of an underlying magnetic bilayer.

The increasing amount of data being processed in today's electronic devices for classification tasks in image and audio recognition, autonomous driving, smart sensors signal processing or machine learning, requires a transition from the conventional compute centric paradigm to a more data centric paradigm. In the classical von Neumann architecture, the data is transferred between computing and memory units via a bus system with limited bandwidth, giving rise to the well-known von Neumann bottleneck. In order to bridge the existing gap between memory and logic units, the concept of physical separation between computing and memory unit has to be repealed.

Ferroelectric Tunnel Junction (FTJ) devices can be applied as synaptic weighting elements in neuromorphic processors, and offer the possibility of massive parallelism (fig. 1). These architectures use artificial neurons and synapses to emulate biological primitives underlying learning. In particular, the synapses act as both storage and computing element. Indeed, their role is to facilitate or inhibit the connection between neurons by changing their weight. In case of FTJs devices, the change of weight is mapped into a change of the device conductance.

In order to use FTJ devices for applications in beyond-von Neumann computing, their properties should be further improved, for example increasing the tunneling current and the tunneling electroresistance ratio. BEOL-compatible processes can be developed to modify device behavior, such as work function engineering of the electrodes for increasing tunneling currents (fig. 2). Additionally, the device operation should be optimized to target specific functionalities and weight update schemes, which requires understanding of the device behaviour.

Novel devices based on spin-orbit interactions offer an alternative route to non-volatile memory devices. Skyrmions in magnetic bilayers can be used for memory-in-logic, with the benefit that they are topologically protected and highly robust. The integration of ferroelectric thin films with magnetic bilayers and device stacks designed for spin-orbitronics (fig. 3) enables investigation into a new generation of highly efficient, low-power, non-volatile components for beyond-von Neumann computing. The eventual target is to enable electric field control of magnetic spin textures.

Cooperation: X-FAB, IBM, IMDEA Nanociencia, CEA-Leti, CSIC, FAU, IUNET, Universities of Udine, Modena, Groningen, Zürich, HZB, NCSRD, ETH Zurich, AMAT, Melexis

Publications: J8, J15, C8, C23, C30

Contact: Dr. Stefan Slesazeck

Reconfigurable Field Effect Transistors

With classical scaling of CMOS transistors according to Dennard 's scaling rules running out of steam, new possibilities to increase the functionality of an integrated circuit at a given footprint are becoming more and more desirable. A promising concept in this sense is to increase the functionality of a system by keeping the number of individual elements the same.

The reconfigurable field-effect transistor (RFET) can provide such a feature, as it is an electronic device whose conduction mechanism can be reversibly reconfigured between n-type and p-type operation modes. In its most versatile variant, three-independent gates are patterned over a nanoscale channel, whereby the two outer gate electrodes directly control carrier injection across the Schottky junctions at source and drain (Fig. 1). The device can be operated either at the source-sided gate or at the central gate, which corresponds to a high-VT, or low-VT mode, respectively (Fig. 2). As both gates are placed in series, the transistor embodies the wired-AND function. Importantly, RFETs do not rely on chemical doping caused by impurities, b ut rather on electrostatic doping, i.e. the generation of mobile carriers via an external potential.

Over the last years, NaMLab has focused on the transfer of this lab technology originally demonstrated on silicon nanowires to more mature industrial processes and materials. Thereto, a robust top-down route for fabrication on SOI substrates using electron beam lithography and reactive ion etching was setup. The gate sizes of the individual devices were adjusted to cover for some variability in the silicide formation. As a result, lab devices can be fabricated with sufficient yield and throughput to perform statistical analysis, first reliability investigations, and the demonstration of functional logic gates. Also, the operation of the devices at high and low temperatures has been investigated.

Moreover, the cross-shape RFET was demonstrated as a radically new device variant based on the of unique transport features of Reconfigurable Transistors. This device utilizes multiple source and drain contacts on a common-body, each being individually gated, thereby facilitating transistor-level current routing through each of its branches, embodying a wired-OR functionality (Fig. 3). Providing linear addition of the current of all sources at the single drain, the device concept has potential for flexible signal routing or neuromorphic circuit applications.

Cooperation: RWTH Aachen, CNRS-LAAS Toulouse, INL ECL Lyon, AMO, TU Wien

Publications: J21, J25, J47, J62, C11, C24, C26

Contact: Dr. Jens Trommer

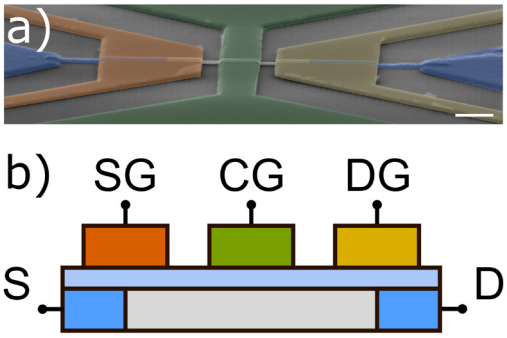


Fig. 1: a) False-colored SEM image of a fabricated RFET (scale bar 200nm). B) Schematic cross section of the same three-gated RFET showing source (S), and drain (D) together with gates aligned to source, drain and in the center of the channel (SG, DG, CG).

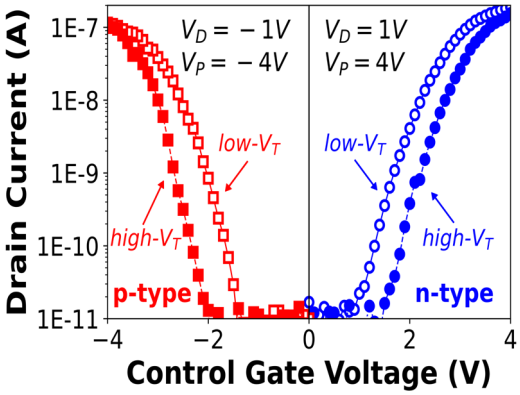


Fig. 2: Measured n-type (blue) and p-type (red) transfer characteristics of a three-gated RFET as shown in Fig. 1. Typically, a high-VT mode is achieved when operated at SG, while a low-VT mode is achieved when steered at the CG. DG is always used for programming.

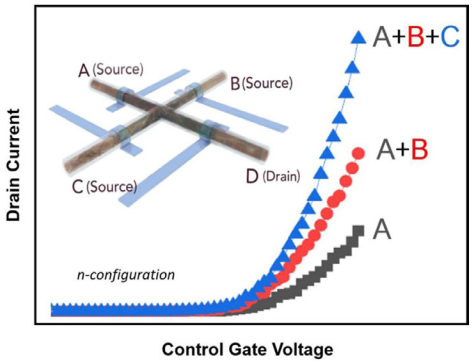


Fig. 3: 3D schematic of the fabricated cross-shape reconfigurable field effect transistor and n-type transfer characteristics with one, two, and three source terminals operating at the same time.

Polymorphic Circuits for Hardware Security Applications

S1	S2	S3	S4	P1	P2	OUT
A	A	A	A	0	1	NOT
A	B	A	B	1	0	2NAND
A	B	A	B	0	1	2NOR
A	B	¬ B	¬ A	1	0	2XOR
A	B	¬ B	¬ A	0	1	2XNOR
A	S	¬ S	B	0	1	2MUX
A	B	A	B	¬ C	C	3MIN
A	B	¬ B	¬ A	¬ C	C	3XOR

Fig. 1: RGATE logic table. Depending on 4 signal and the two program inputs, eight different functions can be mapped with the same four-transistor logic-gate.

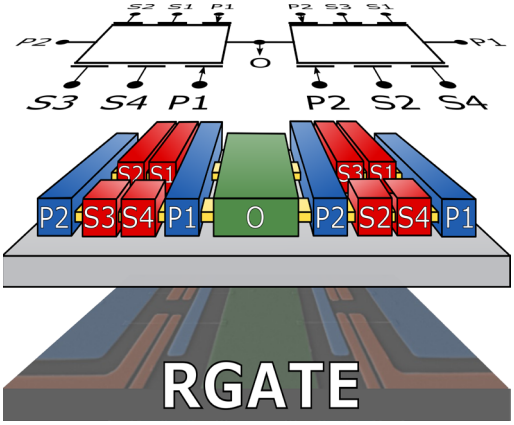


Fig. 2: Illustration of possible non-idealities in a ferroelectric-dielectric bi-layer stack that is researched for stabilization of negative differential capacitance effects.

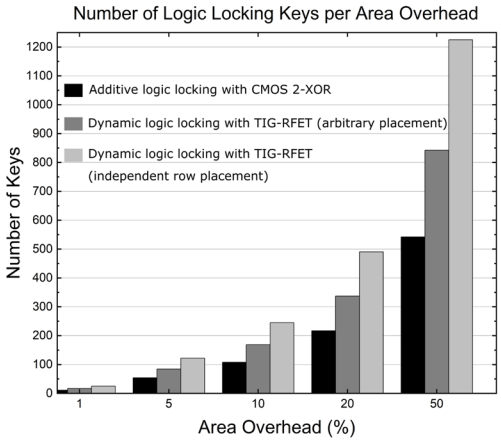


Fig. 3: Logic locking of using RFET logic gates vs. CMOS. Up to 45% more keys can be added per area overhead.

The multiple operation states of reconfigurable FETs open up new opportunities for logic circuit design. Mainly, two features that were previously not accessible with conventional FETs are currently being studied. First, runtime-reconfigurable logic gates can be built, providing multiple functionalities as programmed on-the-fly by volatile select signals. One basic example is given by the compact cell, that can switch from NAND to NOR operation. Distinctly, those cells always operate in a complementary manner, reaching a full swing output and exhibiting the same delay for both functions. The second feature is the integration of multiple gate electrodes along the channel, merging paths of series transistors within a single one, without increasing the internal resistance of the individual device. This feature can be exploited to build efficient XOR and Majority gates. Both features can be combined to yield a logic gate built from four transistors able to map 8 different functionalities (Fig. 2).

This so called RGATE (Fig. 2) shows prominence for hardware security applications, predominantly due to two features: functionality polymorphism and structural polymorphism. Just by looking at the cell layout, it is impossible to retrieve their underlying electrical functionality. This polymorphic nature enables new approaches on hardware security solutions, such as logic locking, camouflaging, physically unclonable functions (PUFs), or chip authentication. Considering careful gate level design solutions, it is even possible to equalize the propagation delay of two related operational modes of a NAND/NOR reconfigurable logic gates, leading to near delay-invariant designs. The remaining differences in the delay traces is well hidden by the influence of process fluctuations, suggesting a high application potential in the field of securing circuits against timing side-channel-attacks.

One particular hardware security option with RFETs is to utilize the dynamic reconfigurable gates for logic locking. Here, instead of inserting additional XOR gates to a circuit design, existing gates are replaced by the polymorphic gates. This way the area overhead can be smaller. Also, it is not possible to strip the logic lock from the original design. First analysis on the ISCAS-85 benchmark have revealed that up to twice the number of keys can be added with this technique to any given design while keeping the same area overhead (Fig. 3).

Cooperation: TU Dresden, TU Darmstadt, KIT, Universität Bremen, GlobalFoundries, TH Mittelhessen

Publications: J20, J43, J61, C7, C9, C16, C29, M2

Contact: Dr. Jens Trommer

Back-Bias RFETs on an Industrial 22 nm FDSOI Platform

One focus of NaMLab's research is the transfer of promising research results into real world applications. NaMLab is currently working together with its industrial partner GlobalFoundries towards to integration of the RFET concept into its 22 nm fully-depleted silicon-on-insulator (FDSOI) platform to serve as potential add-on technology. Here, the structural similarities of RFETs with FDSOI transistors are beneficial for the ease of co-integration. In principle, the same materials and processes can be used and no additional mask sets with critical dimensions are needed.

In this framework a new back-bias (BB) RFET device concept was conceived. Instead of multiple independent front-gates, the inherently present back-gate is used for programming here, leading to demonstration of the worlds smallest RFET with only 20 nm gate lengths and 80 nm width. Most process integration modules are shared with the n-FETs of the baseline technology, such as STI, hybrid etch, gate-first high-k metal gate (HKMG) front gate integration, and the complete BEOL. Modified S/D terminals are used to create silicide-to-semiconductor junctions in close proximity to the doping-free channel region (Fig.1).

In the BB-RFET concept, we exploit the body-bias effect in FDSOI to adjust the carrier transport controlled by the front gate (FG) electrode. Different to other concepts, both front and back gate capacitively couple to the whole channel region. The applied VBB defines which charge carriers are injected to the active region for a given bias point of the front gate. This way, the whole transfer characteristic is shifted reversibly between the three different operation modes: p-type, ambipolar, and n-type. TCAD and Verilog models mimicking the device behavior were created as shown in Fig. 2.

The new device concept is interesting for analog signal processing in wireless communication or integrated sensing systems. For example, a single transistor can be used for frequency doubling by exploiting the symmetric parabolic shape of the ambipolar mode, as illustrated in Fig. 3. By varying the applied back-bias the same circuit can be reconfigured to either signal follower or phase shifter, depending on the selected mode of the RFET. From this concept a single-transistor binary-phase-shift-keying circuit (BPSK) can be derived. Using our simulation models also other single transistor analog building blocks, such as a reconfigurable half-wave and full-wave rectifier have been proposed.

Cooperation: Globalfoundries Fab 1 Dresden, TU Darmstadt

Publications: J33, C10

Contact: Dr. Jens Trommer

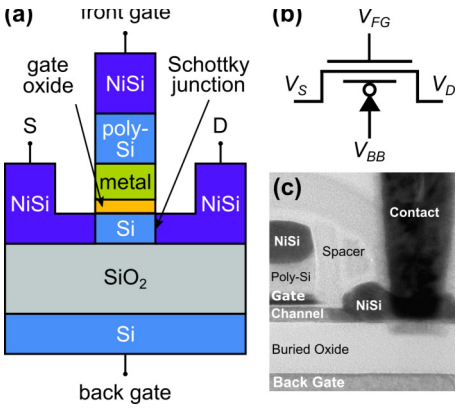


Fig. 1: Sketch of the back-biased reconfigurable transistor (BB-RFET) requiring only one front gate and utilizing the back-bias (BB) for mode selection. NiSi contacts are driven inside the channel.

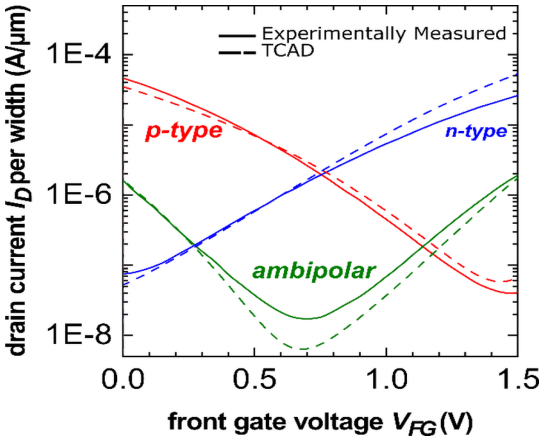


Fig. 2: Measured and simulated transfer characteristics of a BB-RFET with $|V_{DS}|$ = 1.5 V. P-type, n-type, and ambipolar modes are selected by the applied back bias.

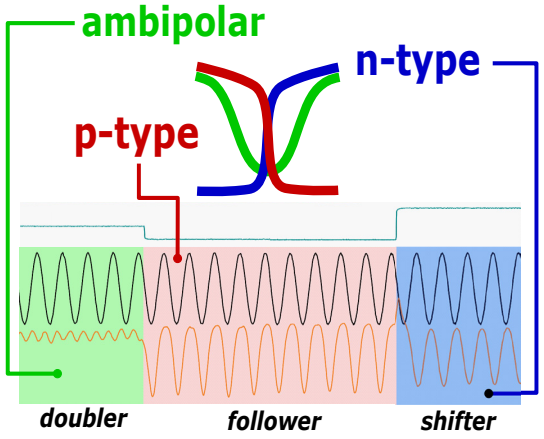


Fig. 3: Three-to-one signal processing with a single BB-RFET. Depending on the applied back bias, a signal follower, phase shifter or frequency doubler is constructed.

Modulation Acceptor Doping for Silicon Nanowires

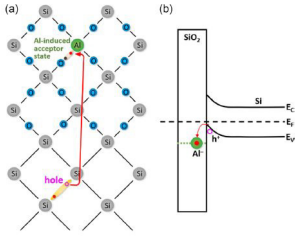


Fig. 1: Schematic illustrations of SiO_2 modulation doping for silicon. (a) lattice diagram of Si/SiO_2 with Al acceptor formed in the dielectric. The red arrow indicates the electron tunneling from Si to the unoccupied acceptor state. (b) Band diagram indicating the different energy levels. the different energy levels.

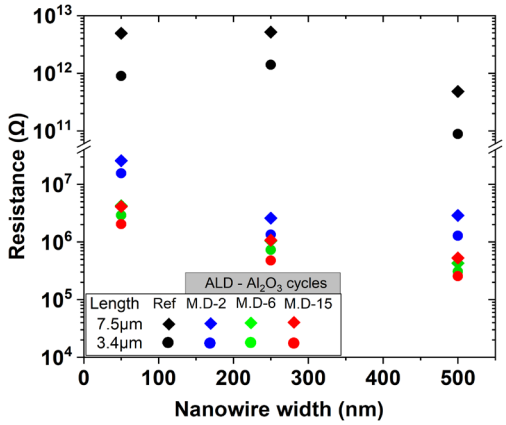


Fig. 2: Measured resistances as a function of nanowire width for three different variations of modulation doped Si nanowires and the reference undoped wires. A reduction in total resistance of more than six orders of magnitude compared to the reference is shown.

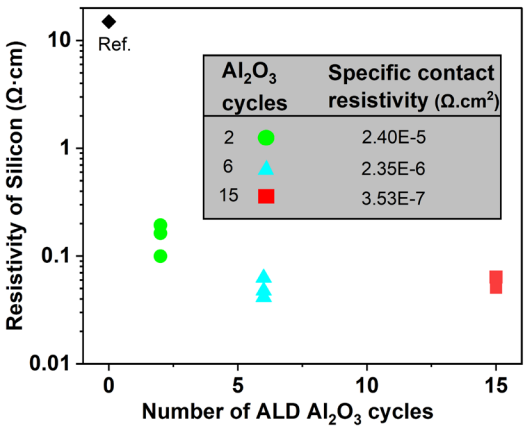


Fig. 3: Result of TLM analysis. Lowering of silicon resistivity via the modulation doping process. Inset shows the reduction in specific contact resistivity for the same variation in ALD Al_2O_3 cycles.

The purposeful introduction of defects within the Si crystal to tune the properties of electronic devices, for example achieving higher conductivity and a lower parasitic source/drain resistance, has always been a fundamental part of semiconductor technology. This process, called doping, is decisive for the functionality of the material that is defined by acceptor (p-type) or donor impurities (n-type). However, these impurities cause a multitude of problems that counteract on the final device performance such as speed, power consumption and efficiency. At the nanoscale, most of these dopants act as scattering centers in the channel that reduce the mobility of the carriers, and are prone to spatial redistribution due to dopant out-diffusion, and statistical fluctuations.

NaMLab is currently working with its research partners to overcome the drawbacks of conventional doping methods at the nanoscale for Si with the concept of Modulation Acceptor doping, with places the defects spatial separated from the channel material. Such a concept was established for silicon nanowires by introducing Al dopants into to the SiO_2 dielectric surrounding. The structural properties of the aluminum (Al) atom acting as an acceptor makes it possible for it to be integrated into the SiO_2 lattice offering an unoccupied energetic state below the valence band of silicon. The provision of this vacant energy level attracts electrons from silicon that are capable of tunneling to the acceptor states, modifying the behaviour of silicon as p-type with holes as dominant carriers (Fig. 1).

The proof of concept for this approach was demonstrated on Si nanowires fabricated from silicon-on-insulator (SOI) wafers. The modulation doping process involves forming a stack of layers mainly SiO_2 and Al_2O_3 on top of the structured nanowire that functionalizes the Si channel after a thermal activation process. The devices were characterized through electrical measurements by forming metal-silicide contacts. A significant reduction in the electrical resistance of the nanowires was reported (Fig. 2) for varying Al acceptor densities in SiO_2. This novel approach has proven to influence both the Si resistivity and the specific contact resistivity that were independently characterized by transfer length measurements (Fig. 3). A carrier density equal to 5E18 cm^{-3} dopant atoms has been achieved experimentally. As for classical doping methods, a broad range can be defined by varying the number of atomic layer deposited (ALD) Al_2O_3 cycles. Also, it has been shown that the charged defects in the shell have an additional effect on the Schottky contact properties of the silicon nanowires. At present, the concept is being further developed for application in Junctionless nanowire transistors.

Cooperation: Technische Universität Bergakademie Freiberg, Australian National University (ANU), Canberra

Publications: J9, J10, J11, C4

Contact: Dr. Jens Trommer

Resistive Switching Devices

The central aim of the research on Resistive Switching Devices is the development of materials and device structures, capable of changing their electrical resistance or capacitance by applying external voltages. The resistive memory device – the so called ReRAM – is one of the potential candidates for the realization of novel memories, since it is characterized by very fast access times, non-volatility, and low power consumption. A further interest for the adoption of these devices - also referred to as memristors - is the application of such reconfigurable devices in neuromorphic nano-circuits, exhibiting the unified functionality of logic and memory in one device. NaMLab's activities cover the deposition and modification of dielectric thin films and electrode layers, the physical and electrical characterization as well as the modeling of the switching properties.

NaMLab's research focuses on niobium oxide (NbO_x)-based resistive switching devices. By variation of the fabrication process, electrode materials and thin film composition a large variety of different switching characteristics could be obtained.

Fig. 1 depicts the measured impedance over frequency of a NbO_x / Al_2O_3 -based bi-layer device. For low frequencies the analogue resistive switching behavior results in a splitting into different impedance states that are determined by the different conductance states representing the stored data. At high frequencies above 10^5 Hz the impedance is mainly determined by the capacitive part which naturally results from the metal-insulator-metal structures. Finally, there is a transition region in which we can observe memcapacitive properties – that is a change of its capacitance depending on the internally stored memory state. The combination of resistive and capacitive switching effects in these devices gives rise to a rich dynamic behavior that we utilize in the conception of novel devices such as neuro-transistors or synapses for unconventional and neuromorphic computing. For example, the data shown in Fig. 2 depicts the potentiation and depression behavior of an artificial synapse for both the memristive and memcapacitive part. Physics-based models that are able to describe the electrical device behavior which are further used in circuit simulation. Finally, we integrate the devices together with transistors as provided by project partner TUD, or manufacture stand-alone cross-bar arrays as shown in Fig. 3.

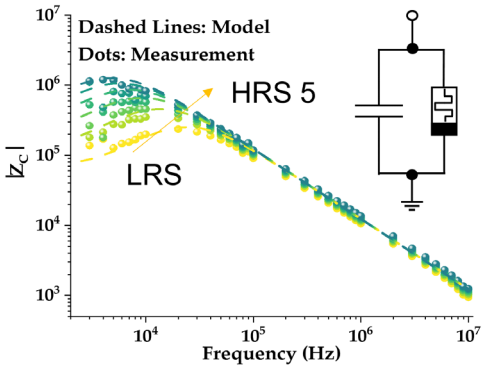


Fig. 1: Measured impedance of an analogue resistive switching device based on a niobium oxide / aluminum oxide bi-layer stack that exhibits memristive and memcapacitive behaviour.

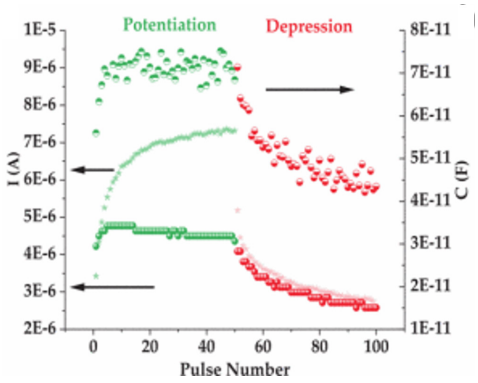


Fig. 2: Measured change in memristance and memcapacitance of an analogue switching device when applying multiple accumulative voltage pulses, showing synaptic potentiation or depression for applications as artificial synapses.

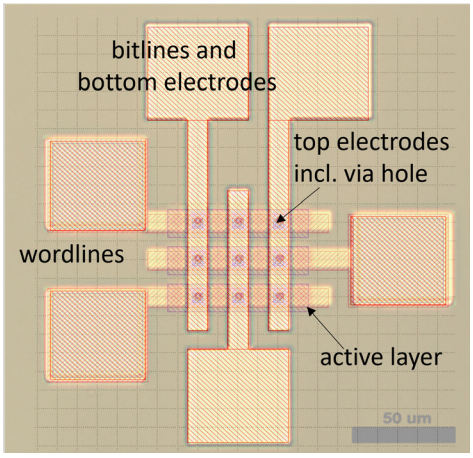
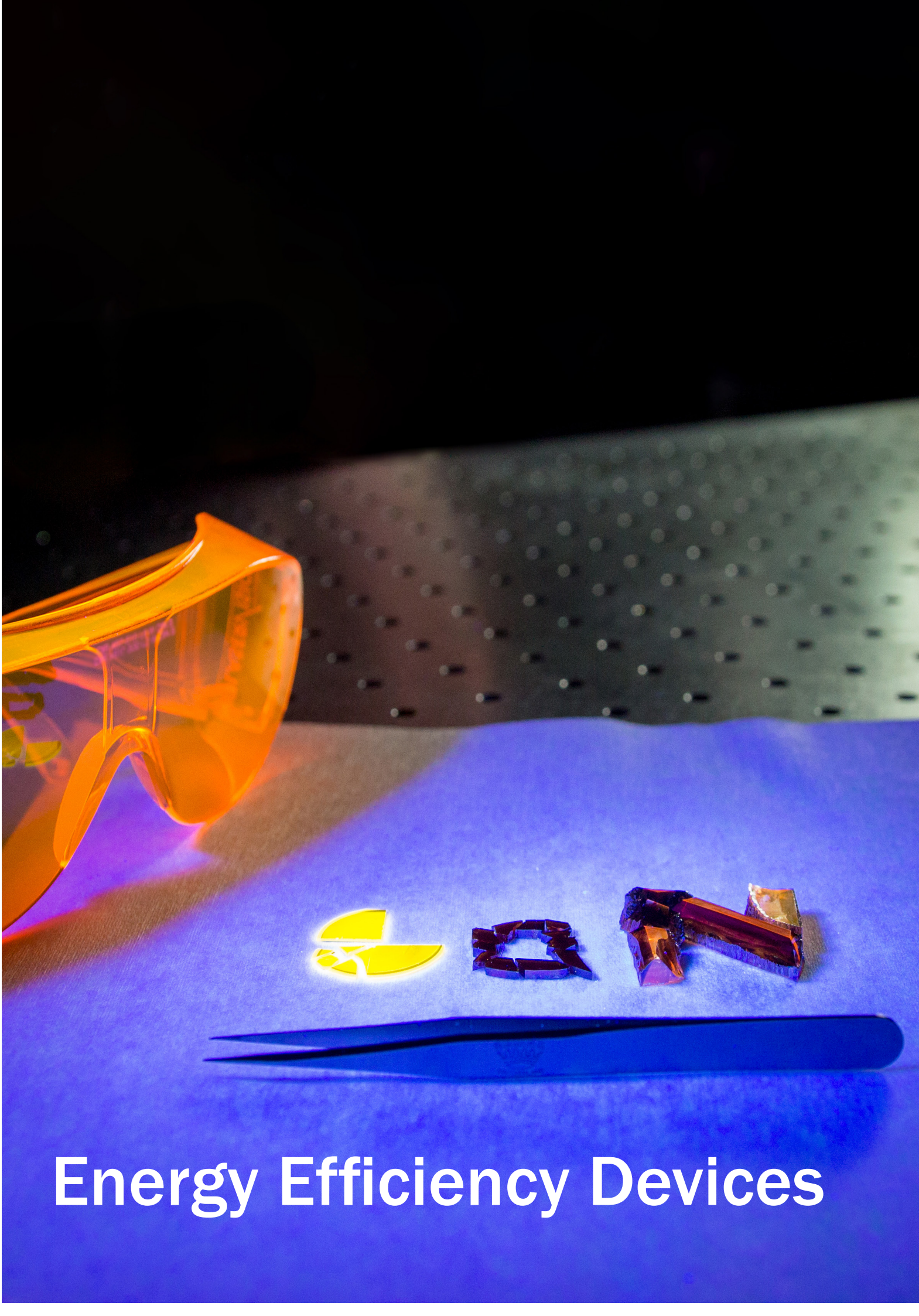


Fig. 3: Overlaid layout and top-down microscope image of a 3x3 crossbar array of analogue switching devices.

Cooperation: TU-Dresden, IHP

Publications: C14, C15, C20

Contact: Dr.-Ing. Stefan Slesazeck



Energy Efficiency Devices

GaN HVPE

Since 2011, NaMLab is belonging to a small but elite group of bulk-GaN growers. It cooperates on-site with Freiberger Compound Materials (FCM) in Freiberg and owns a modified and optimized state-of-the-art vertical HVPE reactor. The focus of the research and development is on the growth of several millimeters thick GaN-crystals (Fig. 1). So far, crack-free 3" crystals can be grown reliably and cut into distinct 2" wafers (Fig. 2). Different dopants are applied to adjust the electrical properties between n-type and semi-insulating. Besides upscaling to higher diameters, the optimization of the lattice properties, e.g. the lattice bow, is of major interest.

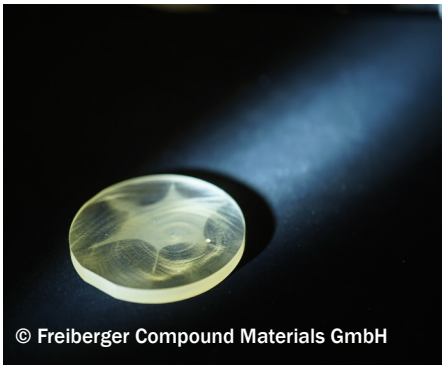


Fig. 1: Unintentionally doped (UID) 2" round-ground GaN crystal grown on a template optimized for self-separation.

Due to the hetero-epitaxial approach of the HVPE process, bowing of the crystallographic lattice planes towards the crystal edge can generally not be avoided. Recent developments of the growth process promise the lattice properties (e.g. lattice radius of curvature) to be competitive to homo-epitaxial approaches.

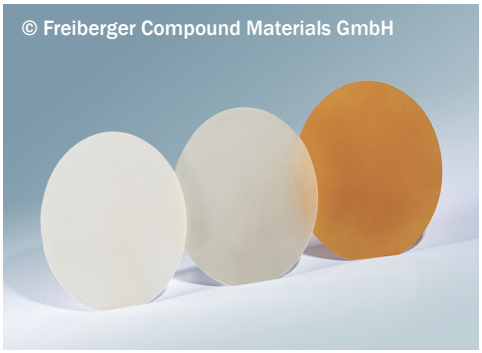


Fig. 2: 2" GaN wafers cut from self-separated, ~5 mm thick boules. From left to right: unintentional doping, n-type and semi-isolating.

N-type conductivity above the unintentional doping level (charge carrier concentrations not larger than 5 x 10^{16} cm^{-3}) is achieved by using Silicon (Si) as a dopant.

On the contrary, semi-insulating GaN crystals have been established by doping with deep acceptors, especially Manganese (Mn) by a solid-state method. High doping concentrations above 10^{18} cm^{-3} are already possible without deterioration of the lattice properties (Fig. 3). Additionally, a bubbler setup using a metal-organic $(MCp)_2Mn$ precursor has been established to improve the flexibility and control of the Mn doping. While the dopant distribution perpendicular to the crystal surface is uniform, there is a large lateral concentration variation for both Mn doping approaches (Fig. 4).

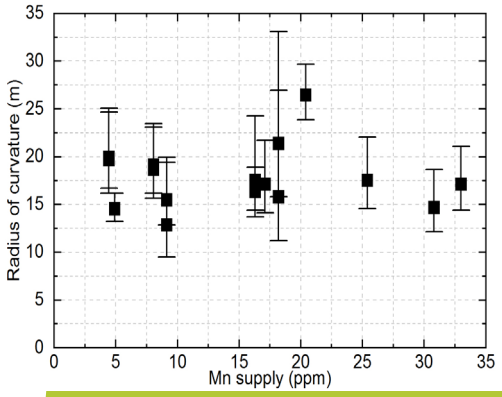


Fig. 3: Crystal lattice radius of curvature as a function of Mn supply for a solid-state doping method.

Future targets are the improvement of the lateral doping homogeneity as well as increasing the doping concentration for the bubbler doping while maintaining the high lattice quality. Furthermore, the suitability of other metal-organic dopants like Cp_2Fe (ferrocene) or DEZn (Diethylzinc) will be evaluated for the fabrication of semi-insulating GaN.

In general, the efforts towards a further improvement of the crystal lattice bow, better understanding of dopants incorporation and increase of the crystal diameter will be continued.

In 2022 a planetary MOVPE reactor owned by NaMLab was installed expanding further the on-site cooperation with FCM. The MOVPE reactor was successfully started up. The development of MOVPE-GaN templates designated to be used as starting seeds in the HVPE GaN crystal growth has started.

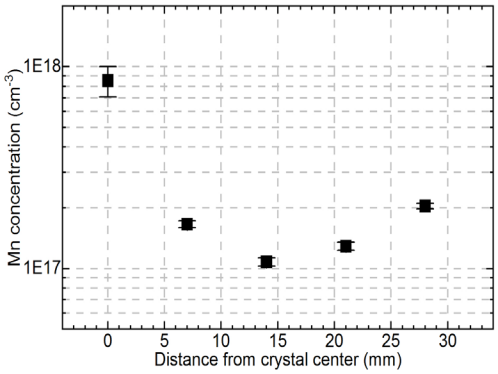


Fig. 4: Mn concentrations measured at equidistant points along a crystal radius for the bubbler doping approach.

Cooperation: Freiberger Compound Materials GmbH (Germany)

Contact: Dr. Friederike Zimmermann

GaN MBE & Fundamentals

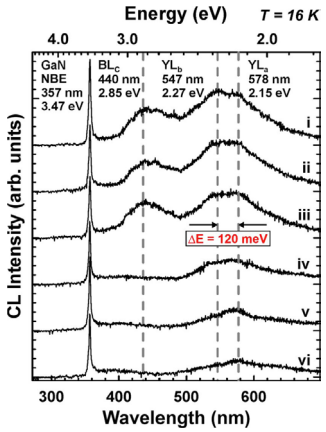


Fig. 1: TEM cathodoluminescence spectra recorded at low temperature from positions in one GaN stack without (regions vi - iv) and with intentional carbon incorporation (i - iii) at a level of 5e17 cm^{-3}. From both regions YL around 2.2 eV is observed. One YL band centered at 2.15 eV is visible from each part of the sample, whereas another band at 2.27 eV is exclusively observed in carbon-doped material. This finding implies that a so far unknown acceptor must be present also in intrinsic GaN, resulting in YL. The blue band around 2.85 eV is exclusively seen in carbon-doped GaN.

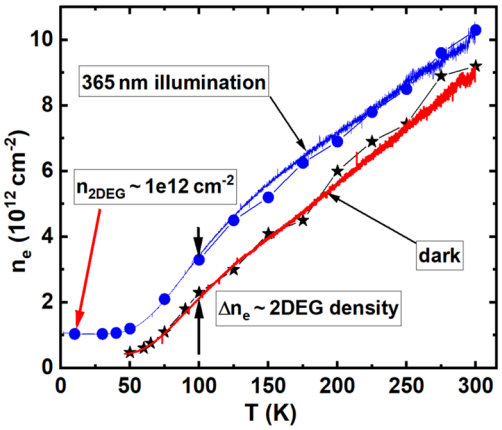


Fig. 2: Temperature-dependent densities of a GaN/AlGaN layer stack extracted from magneto-transport data. The silicon contamination at the substrate/MBE interface was compensated with carbon, which acts as a deep acceptor. At low temperature, the parasitic conductivity resulting form the silicon adhesion at the substrate surface was eliminated. Hall voltage measurements were performed at fixed temperature while sweeping the magnetic field (dots) and at fixed magnetic field while sweeping the temperature (solid lines). Since a 2DEG is only present under UV illumination, the density contributions resulting from the 2DEG and the parasitic channel can be separated.

During the past years the growth of ultra-pure GaN/AlGaN heterostructures with atomically-smooth interfaces and surfaces on bulk GaN by molecular beam epitaxy (MBE) was established. The resulting layer stacks are a perfect reference system for fundamental material investigations as well as a test ground for novel electrical and optical device concepts. In particular, the role of carbon incorporation in GaN was re-visited. Carbon is a deep acceptor in GaN and historically considered to result in an impurity band around 2.2 eV in photoluminescence studies, known as yellow luminescence (YL). Several years ago, it was already realized, that YL is also detected from GaN with no or a low level of incorporated carbon. Cathodoluminescence investigations at low temperature inside a transmission electron microscope (TEM) revealed, that two YL bands can be detected from carbon-doped GaN, while one around 2.15 eV is also present for intrinsic material (Fig. 1). YL results from carbon incorporation, but in intrinsic material there must be a hitherto unknown deep acceptor present, which also results in a YL band. This unknown deep acceptor has a similar binding energy as carbon, reflected in the difference of 120 meV between the two YL bands.

GaN/AlGaN stacks hosting a two-dimensional electron gas (2DEG) are the prerequisite for lateral field-effect transistor (FET) operation. Parasitic conduction paths in these stacks deteriorate FET performance, since the 2DEG cannot fully be depleted and thus the transistor cannot be turned off. Parasitic conductivity results from silicon at the substrate/MBE interface and originates from the adhesion of particles when the substrate is exposed to ambient atmosphere prior to loading for the subsequent overgrowth. Silicon acts as a shallow donor in GaN and the resulting free charges could in principle be compensated by a deep acceptor. In the present case, a carbon layer at the substrate/MBE interface was introduced to compensate the parasitic conductivity. It was shown that at low temperature the 2DEG is the only conducting channel and any parasitic conduction path was suppressed (Fig. 2). In this specific layer stack, the 2DEG is only present under illumination with ultra-violet (UV) light. Thus, magneto-transport measurements performed in the dark and under UV exposure allow for the separation of the density contribution from the 2DEG and the parasitic channel. Further it was demonstrated, that the density difference in the dark and under UV exposure is constant over the entire temperature range and thus the 2DEG density does not depend on the temperature.

Cooperation: MPI CPfS, Otto-von-Guericke Universität Magdeburg, IHM

Publications: J6, J34, J38, J39, J66

Contact: Dr. Stefan Schmult

GaN-based device technology

The III-V compound semiconductor Galliumnitride (GaN) has outstanding intrinsic material properties for power device applications. NaMLab's GaN device development is focused on electronic power devices with high voltage operation. The High-Electron-Mobility-Transistor (HEMT) concept features a 2 dimensional electron gas (2DEG) at the $Al_xGa_{1-x}N$/GaN heterojunction interface. It represents the backbone of GaN power transistors with planar or lateral current conduction close to the wafer surface. The material for industrial device fabrication consists primarily of MOCVD grown GaN on Si(111) substrates with diameter of 200 mm.

A HEMT technology based on contact lithography for 150 mm wafers is utilized for material characterization and device development in co-operation with external partners (Fig.1). NaMLab is working on process modules for improving overall device performance, stability and reliability. We investigate the integration of a high-k dielectric material underneath the gate electrode to fabricate a Metal-Insulator-Semiconductor (MIS)-HEMT. Process engineering on the (Al)GaN surface prior to the deposition of the dielectric as well as post-annealing of the gate structures improves importantly the threshold voltage stability. An alternative ohmic contact module based on Ta/Al metal bilayers was investigated and compared to the mainstream Ti/Al/Ni/Au contacts. Material engineering resulted in low-resistance Ta/Al/TiN-ohmic contacts (R_c < 1 Ω.mm) at much lower annealing temperatures (≤ 600 °C), which are gold-free and enable a higher integration flexibility. Currently, we explore the integration of ferroelectric materials in the gate architecture of HEMT devices aiming to tune the threshold voltage in dependence of the spatial orientation of polarization, comparable to Silicon-based ferroelectric field-effect transistors.

Another device concept is related to vertical GaN power devices, having the advantage of an almost area-independent scaling of the breakdown voltage. NaMLab has developed a vertical GaN MOSFET device with trench gate configuration and device channel along the vertical sidewall of the trench (Fig 2.). The process integration has been adapted to full vertical devices on 2-inch free-standing GaN substrates with backside contact. Power demo-devices with multiple gate trenches connected in parallel showed threshold voltage > 3V and low specific on-resistance of 3 mΩ.cm². Utilizing a low doped drift layer with thickness of 10 µm and a conformal gate dielectric of 45 nm Al_2O_3, the MOSFET exhibits a pre-mature breakdown at 450 V most likely in the trench corners (Fig. 3). Contrarily, the lateral device termination with field plate structure on the device mesa isolation shows non-destructive breakdown at 1.1 kV.

Cooperation: Freiberger Compound Materials (FCM), X-FAB, TU Dresden IHM, TU-BA Freiberg.

Publications: J29

Contact: Dr. Andre Wachowiak

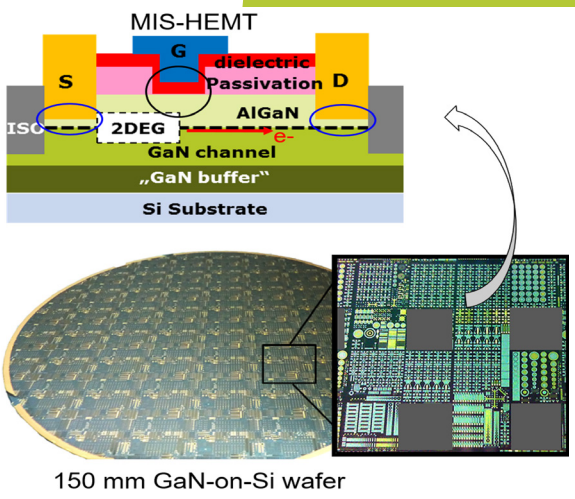


Fig. 1: Cross section MIS-HEMT device, process modules under investigation marked with circles. Below: image of processed 150 mm GaN-on-Si HEMT wafer with zoom into test chip die.

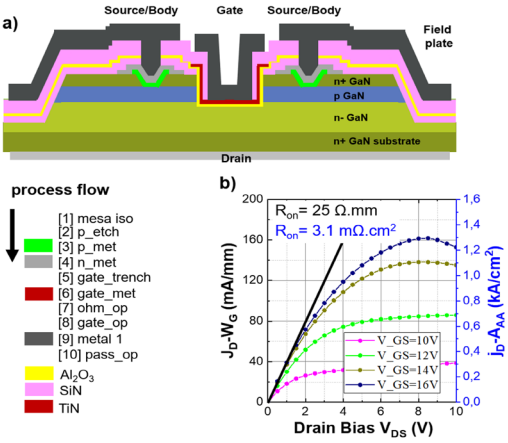


Fig. 2: a) Schematic cross section of trench gate MOSFET with process flow sketch. b) Output characteristics at different VGS and on-state resistance scaled to gate trench width (left axis) and device active area AA (right axis).

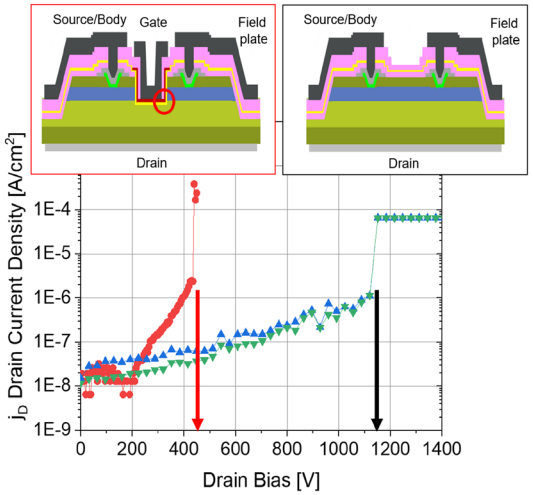
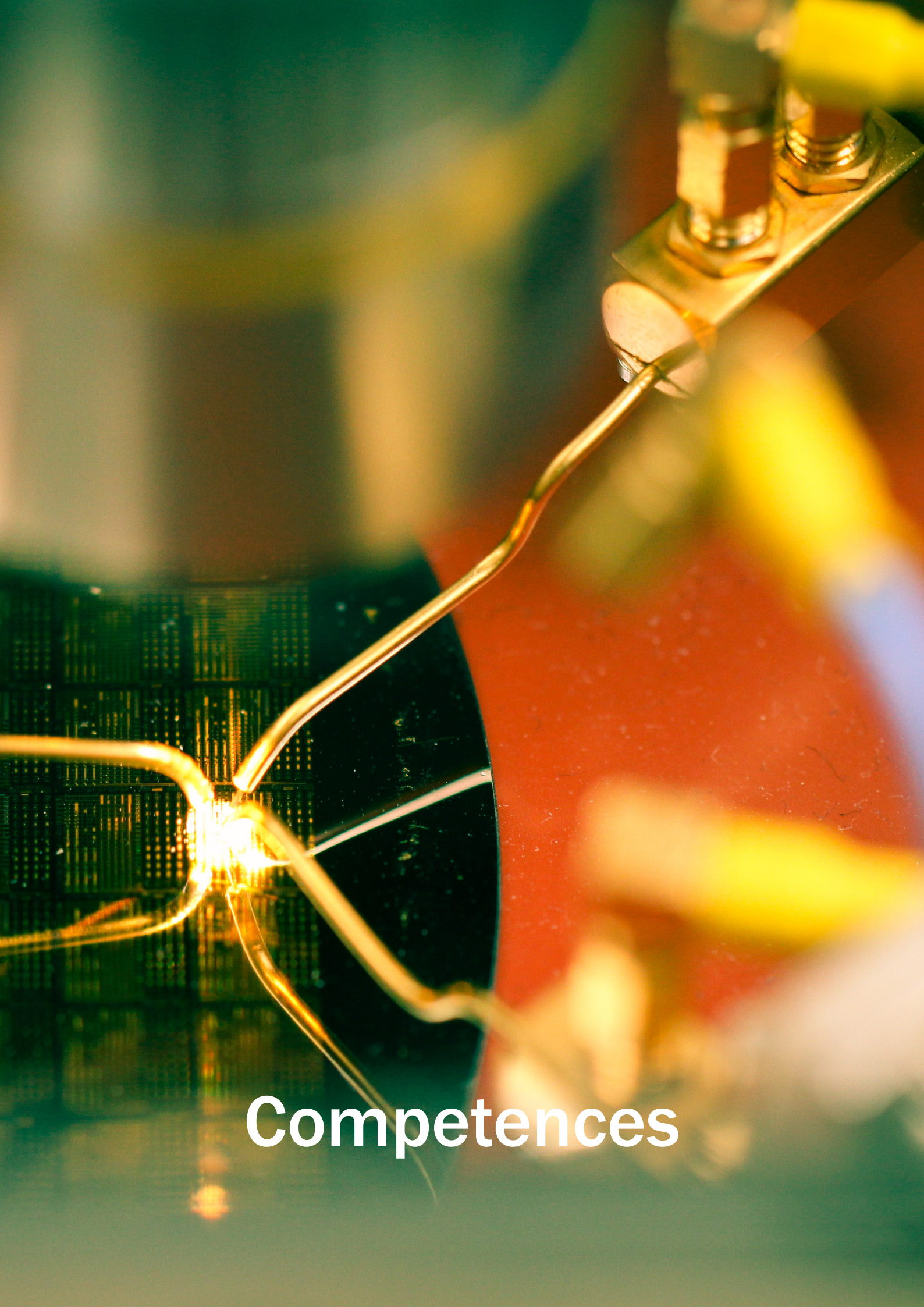


Fig. 3: Breakdown measurements with top electrodes grounded of MOSFET device and test structure with same device layout, but without gate module. Both devices have a field plate on the edge termination. The drain current is normalized to the total device active area AA~1.5*10⁻³ cm².



Competences

Electrical Characterization

Electrical measurements are essential for the characterization of the materials that are used to create electronic devices and circuits. NaMLab adopts a broad spectrum of electrical measurement techniques and analysis methods for device characterization. This includes capacitance measurements, such as C(V), C(T) and C(f), current measurements with down to femto-ampere resolution at temperatures between 5 K and 450 K and voltages up to 3000 V. Samples can be analyzed by direct probing on wafer level using single probes, probe cards or special RF-probes. Package level testing can be performed for long-term reliability characterization or for the adoption of our devices in test-circuits. In addition, carrier lifetime measurements are available on substrates with Microwave Detected Photoconductivity.

The established methods at NaMLab include:

- Analysis of single devices (logic and power transistors), circuits or memory cells by static and pulsed measurements
- Determination device characteristics by C-V and I-V measurements
- Determination of doping profiles by scanning spreading resistance Microscopy (SSRM)
- Reliability characterization of dielectrics, devices and circuits
- Defect characterization by charge pumping and charge trapping analysis and defect spectroscopy
- Measurement of charge carrier mobility with Hall and split-C(V)
- Pulsed and high frequency measurements
- Development of novel characterization methods and test structures

Characterization of memory arrays closer to system level are performed to develop new application scenarios. Fig. 1 shows a packaged 64kBit FeFET memory test chip. It was designed for the investigation of radiation hardness of this technology at UZL in Leuven, Belgium.

In another work, special operation modes such as target programming for analogue and multi-level state storage in conventional FLASH memory arrays were investigated, targeting at the realization of analogue vector matrix multiplication in FLASH-arrays. Fig. 2 shows the measured distribution of on-currents of 720 SONOS cells programmed to eight different levels.

Finally, based on a novel RF-characterization methodology the impact of self-heating effects on the reliability of 22nm FD-SOI transistors was investigated. Fig. 3 shots the extracted thermal resistance of a MOSFET device structure depending on its layout – in this case the number of gate fingers.

Contact: Dr. Stefan Slesazeck

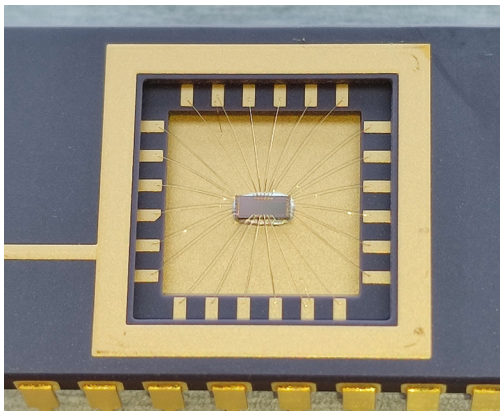


Fig. 1: Packaged 64kBit FeFET memory array for characterization of radiation hardness of this memory technology.

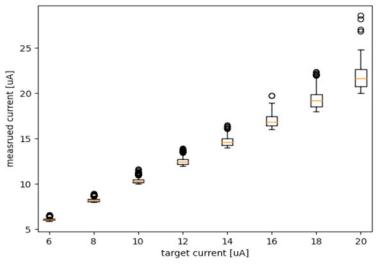


Fig. 2: Measured cell current distribution of 720 SONOS cells after multi-level programming operation targeting at eight different states.

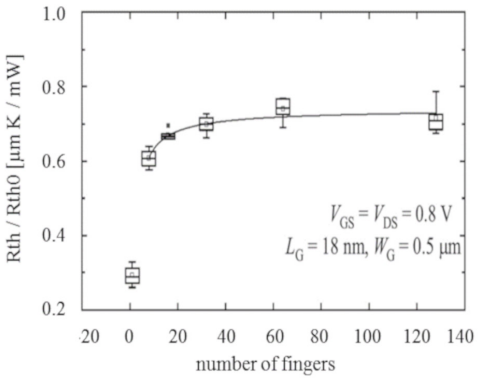


Fig. 3: Measured thermal resistance Rth as a function of the number of gate fingers nf in 22nm FD-SOI transistors.

Physical and Optical Characterization

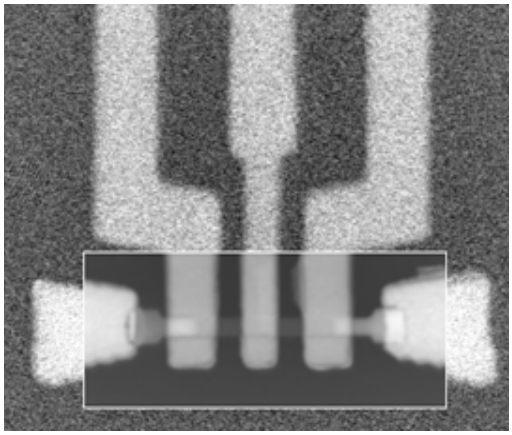


Fig. 1: SEM image of NiSiX contacts below metal gates imaged with an AsB detector.

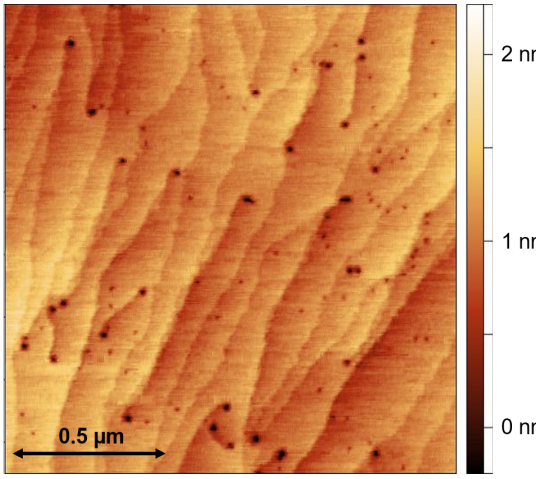


Fig. 2: Surface topography of MOCVD GaN with mono-layer stepped terrace structure. Pits of shallow (deeper) depth indicate end points of threading edge (screw + mixed) dislocations.

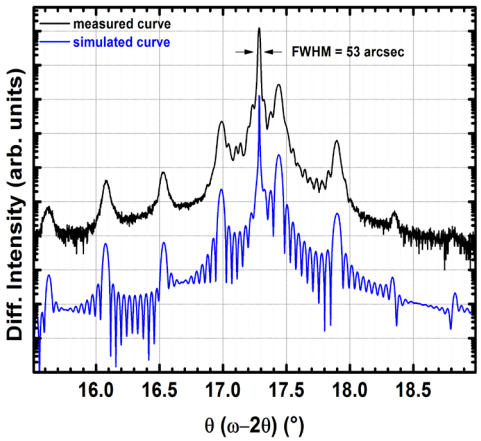


Fig. 3: Measured and simulated high resolution X-ray diffraction pattern of AlGaN/GaN superlattices grown by molecular beam epitaxy at NaMLab.

NaMLab hosts a dedicated physical characterization toolpark to supple-ment its core expertise in state-of-the-art material development and electrical characterization. One focus of the physical characterization at NaMLab aims to provide fast-feedback to the technology development in the cleanroom and at research partners.

Two high-resolution scanning electron microscopes (HR-SEM) are capable of providing high magnification images down to 10 nm resolution. Our new angle-selective-backscattered electrons detector (AsB) allows to obtain superior material contrast with respect to conventional imaging. Moreover, high channelling contrast can also be achieved, yielding more detailed crystallographic information. A possible application is the localization of nickel silicide junctions placed below metal gates shown in Fig. 1. The high material contrast delivered by the detector allows to precisely image the sharp junctions without saturation of the signal by the electron contribution coming from the overlying metal gates. Furthermore, one SEM is equipped with an energy-dispersive x-ray (EDX) detector to reveal chemical composition of the samples covering almost the entire periodic table. The EDX system is coupled with a newly-acquired Electron Back-Scatter-Diffraction (EBSD) detector, to also yield localized in-formation about crystal structure, phases and textures of nanoscale materials.

The atomic force microscope (AFM) is routinely used for mapping the surface topography by using contact or tapping mode. Resolution in the order of 2 nm in the scanning direction (X/Y) and below 0.1 nm perpendicular to the scanning direction (Z) can be realized, shown at an example of an epitaxial grown GaN surface in Fig. 2. At NamLab a big variety of special measurement technique is used with a great expertise such as scanning Spreading Resistance Microscopy (SSRM) to map the spatial dopant distribution, conductive AFM (C-AFM) for measuring local leakage current density, piezo force microscopy (PFM) for analyses of piezo-electric materials by measuring the vertical displacement of the AFM tip in response to an electrical excitation of the sample.

A multifunctional X-ray diffractometer (XRD) is used to yield information about crystal structure. The tool has a resolution of < 40 arcsec and is used for phase analysis, measuring reciprocal space maps, determining the composition of alloys, layer thickness and stress state. A high-resolution X-ray diffraction measurement on a AlGaN/ GaN superlattice structure is shown in Fig. 3.

Cooperation: Freiberger Compound Materials (FCM), X-FAB, TU Dresden IHM, TU-BA Freiberg.

Contact: Dr. Jens Trommer / Dr. Andre Wachowiak

Services

Most of NaMLab technologies are available for services. E.g., the research programs at NaMLab require very specific preparation of samples. The sample preparation ranges from low-complexity approaches of 1D layer stack depositions up to complex BEOL-post processing of functional devices on top of CMOS substrates using up to 5 lithography steps.

This preparation can include deposition of thin films and layers, thermal treatment of samples, patterning by lithography and etching, as well as sample cutting, grinding, polishing and engravings. For this purpose, the 330 m² ISO class 6 cleanroom facility includes various types of deposition tools: physical vapor deposition (PVD), atomic layer deposition (ALD) (Fig. 1), chemical vapor deposition (CVD), and molecular beam epitaxy (MBE). Post deposition anneals can be performed up to 1200 °C for fast anneals. There are fast ramping Rapid Thermal Processing machines available as well as furnaces for long-term treatment. Structures in the range of micro- and nanometers can be manufactured by employing shadow masking and lithographic methods like electron beam (Fig. 2) and laser lithography. The removal of the material includes wet chemical and reactive ion etching (RIE).

Additional processing requirements are adapting wafer geometries, chip dicing and creation of process compatible gadgets e.g. for sample handling. Therefore, NaMLab provides several tools to meet these requirements. A laser cutter is located in NaMLab's clean room. It offers the possibility to process wafers with diameters up to 300 mm and substrate thicknesses up to 1 mm. Via a CNC based vacuum chuck any 2-dimensional shape can be produced. This technique is used for dicing silicon wafers or cutting out small pieces without destroying processed and reusable wafers.

For cleaning and wet chemical treatment of samples, NaMLab owns four wet benches equipped with overflow basins (Fig. 3). They are located in an ISO class 5 cleanroom. Ultrasonic and megasonic tools for mechanical supported surface cleaning in deionized water are in operation. Also cleaning steps like RCA clean and selective material etching can be performed.

Tool overview (excerpt):
Sample and Wafer Processing by Atomic Layer Deposition for metals and oxides, Chemical Vapor Deposition, Sputter Deposition, Molecular Beam Epitaxy, Reactive Ion Etching (RIE, ICP), Rapid Thermal Annealing, Laser Lithography and Electron Beam Lithography
Analysis by Atomic Force Microscope, Ellipsometer, X-ray, SEM with EBSD and EDX
Electrical Characterisation by semi-automated and full-automated (300 mm) prober systems

Contact: Dr. Alexander Ruf

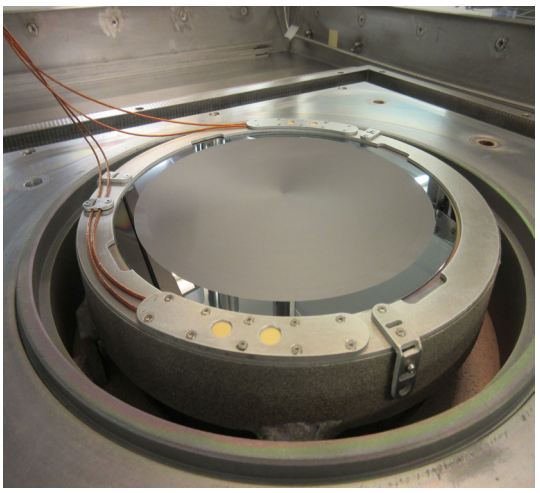


Fig. 1: A wafer loaded in the Oxford Instruments opAL ALD system.

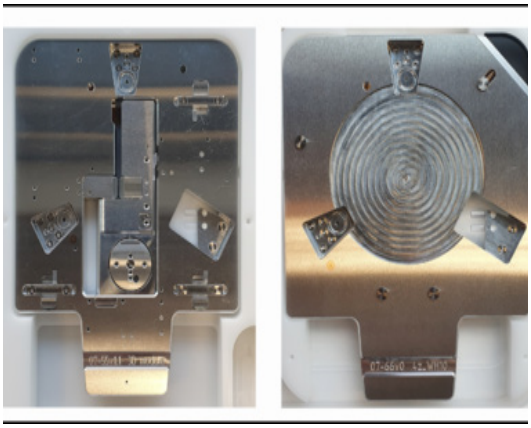


Fig. 2: The Raith eLINE Plus E-beam lithography sys-tem includes a 3D module stage and a 4-inch wafer holder for lithography on different types of samples.

Fig. 3: Various possibilities to perform controlled wet chemical and reactive ion etching.

Facts & Figures

NaMLab main building.

NaMLab in Numbers

Annual Budget

The annual budget over the past six years reflects that NaMLab gGmbH has established itself as an institute with full operating capacity. Further growth of the research institute is limited by the available office space. The turnover has increased slightly and reached about 4 Mio. Euro and is stable overall. The total budget of publicly funded projects and contract research has increased slightly over the last two years. Funding from government sources has reached a base level and is increasing slightly. Government funding accounts for approximately 15% to 20% of total revenues.

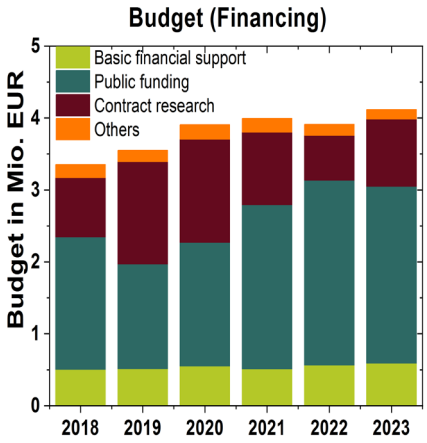


Fig. 1: Annual budget NaMLab gGmbH. The turnover is stable and limited by the available office space.

Investment Budget

The cleanroom facility at NaMLab is conform to the highest standards of microelectronics. 250 m² of class 6 and 50 m² of class 5 clean room (EN ISO 14644) are available for experimental work. With its core competence in materials development, NaMLab runs several deposition techniques such as evaporation, molecular beam epitaxy, sputtering, chemical vapor deposition and atomic layer deposition. A total of fifteen processing tools are used for research. A wet chemistry area is equipped with cleaning, etching and spin coating processes. Two state-of-the-art electrical characterization laboratories for material and device characterization are equipped with 200 and 300 mm wafer probe stations. Additional optical and physical characterization labs are available. In addition, NaMLab has chartered a laboratory in Freiberg, a city near Dresden, which houses a hydride vapor phase deposition tool and a metal organic vapor phase epitaxy GaN deposition tool dedicated to GaN crystal growth research and future GaN device development.

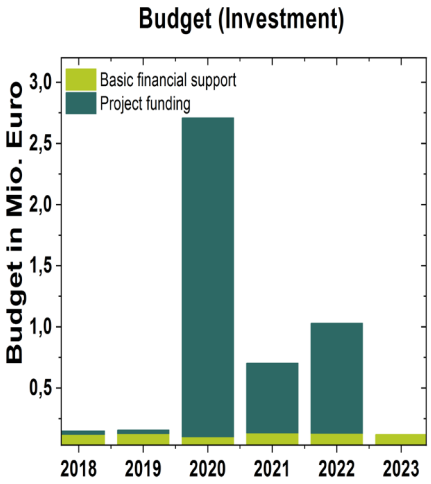


Fig. 2: Invest budget NaMLab gGmbH. The significant investments in the years 2020 to 2022 have been realized by an infrastructure project financed by the European Fund for Regional Development EFRD of the European Commission and by the Free State of Saxony out of the budget approved by the Saxon State Parliament.

The main investment in recent years has been an infrastructure project financed by the EFRD Fund of the European Commission and the Free State of Saxony from the budget approved by the Saxon State Parliament until 2022. As a result of this project, an e-beam lithography writer for processing small samples, an atomic force microscope for various types of surface investigations, a vacuum rapid thermal processing furnace, a fully automated probe station combined with high-frequency measurement capability, a high-temperature chemical vapor deposition system, and an atomic layer deposition tool are increasing the processing capabilities in the NaMLab clean room and laboratories. In addition, a Metal-Organic Vapor Phase Epitaxy GaN deposition tool is now in use at the Freiberg outpost. In addition, NaMLab has invested in the last two years in upgrades for deposition tools, IT hardware and software, and office buildings, all of which were funded by the Free State of Saxony from the budget approved by the Saxon State Parliament.

Employment Numbers

By 2023, the total number of staff employed had reached 40. This includes 4 administrative staff, 3 technical support staff and 5 senior scientists. 17 scientists had planned to submit a Ph.D. thesis. Technicians and Senior Scientists ensure an excellent and stable scientific and technical knowledge base of semiconductor devices, technology and materials for current and future projects.

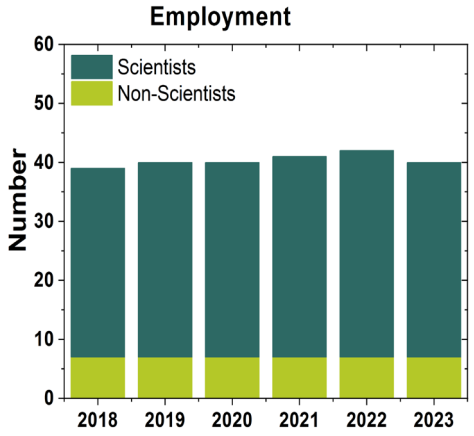


Fig. 3: Employee number development NaMLab gGmbH. In 2022/2023, the number of employees has been stable. The number of master theses, project and semester works is stable too (not shown).

Projects

Europäische Union

BeFerroSynaptic (871737)

BEOL technology platform based on ferroelectric synaptic devices for advanced neuromorphic processors

FvIIMonti (101016776)

Ferroelectric Vertical Low energy Low latency low volume Modules for Neutral network transformers in 3D

Memriness (101042585)

Memristive Neurons and Synapses for Neuromorphic Edge

Crossbrain (101070908)

Distributed and federated cross- modality actuation through advanced nanomaterials and neumorphic learning

FIXIT (101135398)

Scaled FerroelectrIc X-bars for AI-driven sensors and actuaTors

Bundesministerium für Wirtschaft und Energie

ZIM Zentrales Innovationsprogramm Mittelstand

Falcon (ZF4737101AG9)

Flash lamp based activation of passivating contacts for highly efficient solar cells

GaNESIS (16ES1090)

AlN/GaN epitaxy on silicon using reactive plus magnetron sputtering

KaSiLi (03XP0254C)

In-situ Raman investigations on anodic protective layers of silicon- and lithium-based anode materials

KI-IoT (16ME0093)

Holistic open-source platform for embedded system-on-chip

CirroStrato (16ME0210K)

Novel reconfigurable transistors for know-how protection of electronic components

Nitrides 4-6G (16KISK133)

Nitride-based dispersion-lean and efficient millimeter wave devices for future radiation-hard satellite communication technology

Bundesministerium für Bildung und Forschung

ECSEL Joint Undertaking

Ecsel UltimateGaN (826392/16ESE0422S)

Research for GaN technologies, devices and applications to address the challenges of the future GaN roadmap

Ecsel All2GaN (101111890/16MEE0290)

Affordable smart GaN IC solutions as enabler of greener applications

Freistaat Sachsen

LiTRa (100611332)

Development of an insitu Raman measuring station for the determination of temperature-dependent degradation mechanisms in Li- based batteries

EUProNet (100685330)

Ferrroelectric Tunneling Junctions (FTJ) for application as analog memory devices

Freistaat Sachsen

This project is financed by tax funds on the basis of the budget adopted by the Saxon state parliament.

Projects

HiMGaN (MI 1247/15-1)

Exploration of novel electrical and electro-optical device concepts and fundamental physical effects in high-quality wide-band-gap semiconductor hetero structures

Homer (MI 1247/16-1)

Ferroelectric Hafnium Oxide Material Enhanced Reliability

Zeppelin (MI 1247/17-1)

Ferroelectric zirconium oxide for piezo- and pyroelectric devices

SoGraph (MI1247/18-1)

Spin Orbit functionalized Graphene for resistive-magnetic Memories

SecuReFET (MI 1247/19-1)

Secure circuits through inherent reconfigurable FET

BioMCross (SL 305/1-1)

Bio inspired Memcomputing via Crossbar Structures

ReLoFEMRis (SL 305 /2-1)

Reconfigurable logic and multi-bit in-memory processing with ferroelectric memristors

FeDiBiS (SL 305/3-1)

Polarization Switching Kinetics in Ferroelectric/Dielectric Bi-Layer Structures

WUMM (MI1247/24-1)

Wurtzite Solid Solutions as a New Material Class for Ferroelectric Microelectronics

D3PO (SCHR 546/3-1)

Dopant and Defect Physics for Device Optimization for Hafnium Oxide based Devices

PARFAIT II (MI 1247/22-3)

Power-aware Ambipolar FPGA Architecture II

MADSiNano (MI 1247/23-1)

Modulation-Acceptor Doping of SiO2 as Novel Doping Method for Silicon Nanowires

Funded by

DFG Deutsche Forschungsgemeinschaft

German Research Foundation

FreiGaN (100356328)

Development of free-standing GaN wafers with improved homogeneous properties

GaNHoch-VFT (100364091)

Equipment GaN on GaN high voltage and high frequency transistors development

LeistungsSchaltER (100687609)

Power transistors as a switch set

TemCrysT (100686667)

GaN templates, GaN crystals and GaN wafers for the development of vertical GaN transistors

Co-financed by the European Union

This project is co-financed by tax funds on the basis of the budget adopted by the Saxon state parliament.

NaMLab Goes Public

Fig. 1: Long Night of Science 2022. Visitors enjoyed a beautiful evening at NaMLab, got inspired by nanoelectronics science, and learned how to dress for the cleanroom.

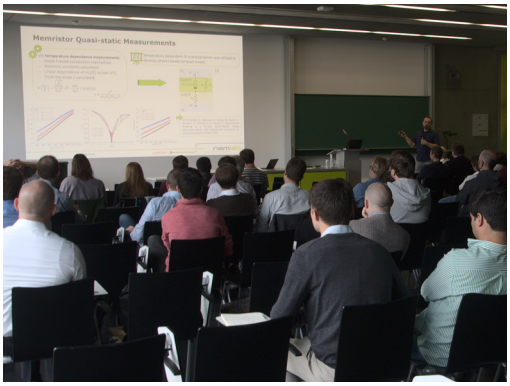


Fig. 2: Namlab High-k Application Work-shop September 2022
First organization in presence after the COVID-19 pandemic in a lecture hall of the TU Dresden.

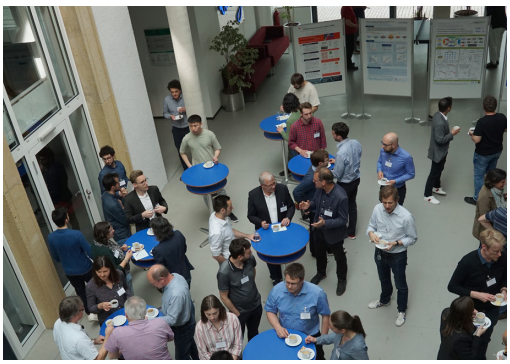


Fig. 3: Namlab High-k Application Workshop 2023
Break between lectures at the Leibniz Institute for Solid State and Materials Research Dresden.

After the COVID-19 pandemic, more and more events came back into the presence. At the beginning of 2022, NaMLab renewed its efforts to make scientific research in nanoelectronics accessible to the public in general, and in particular to inspire young people studying science or engineering. In 2022 and 2023, NaMLab researchers participated as mentors in the annual work experience for 7th and 8th grade students of the Martin-Andersen-Nexö secondary school in Dresden.

Long Night of Science 2022

On July 8, 2022, research institutes, companies and four universities opened their laboratories and lecture halls and offered a comprehensive program for the 19th Long Night of Science. At NaMLab, people got acquainted with material research for future electronics. The program offered guided tours through the laboratories and presented typical characterization methods in experimental shows. Places were set up for young scientists to gain experience in soldering small circuits.

International Memory Workshop 2022

The 2022 edition of the International Memory Workshop (IMW) was organized as a hybrid event in Dresden from May 15 to 18, with NaMLab as one of the local organizers. Half of the participants came from Asia and attended mostly virtually, while the other half from Europe and the USA were able to meet mostly on-site. After the event in Dresden had been planned twice as a onsite event and then switched to virtual due to the COVID-19 crisis, Prof. Mikolajick was happy to welcome about 300 participants in Dresden and another 300 online.

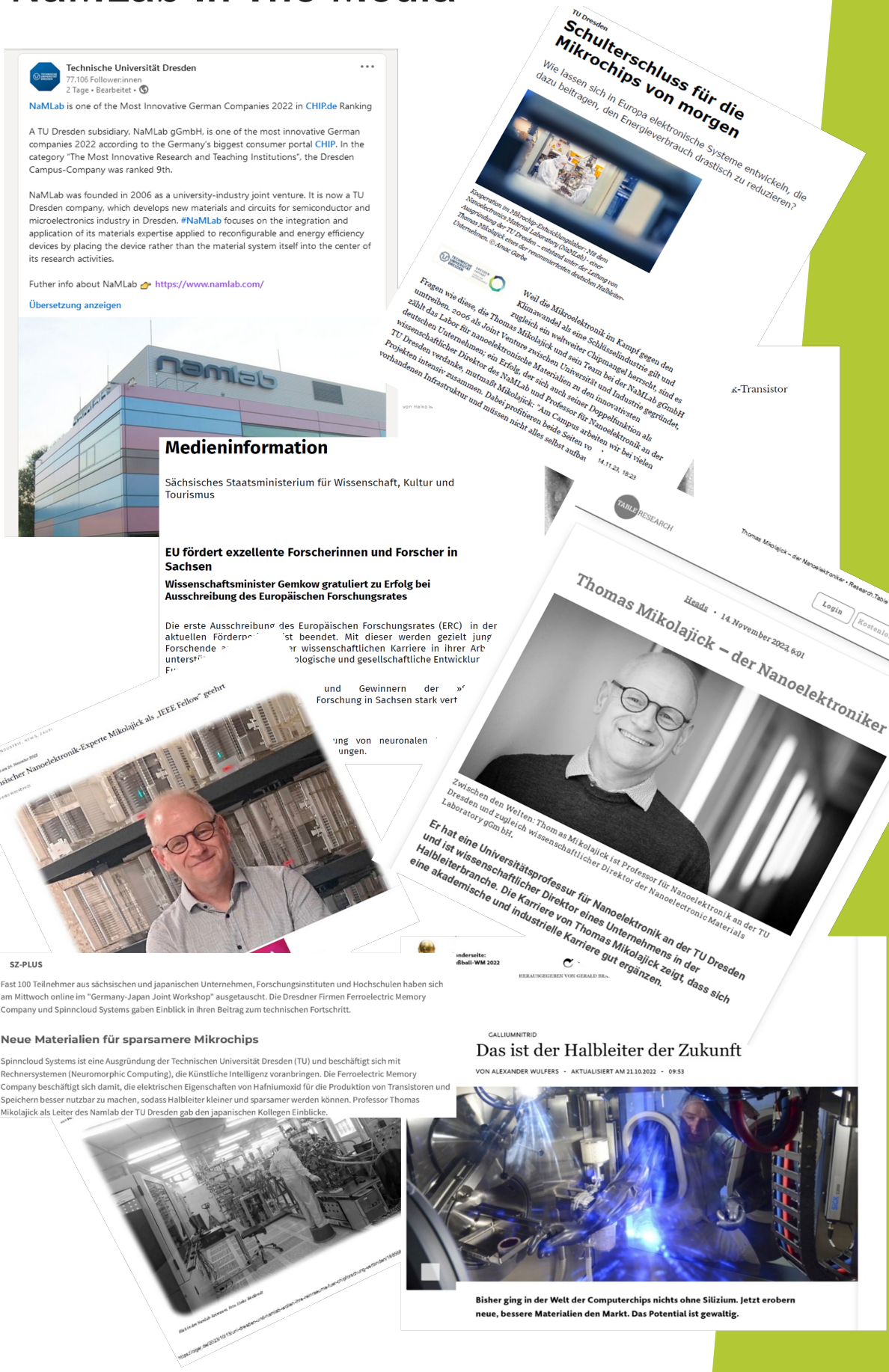
Novel High-k Application Workshop 2022/2023

In 2022, the Novel High-k Application Workshop was organized in two events. First in a six-week series starting on April 23rd with three live online presentations with Q&A session and second in a two-day event on September 12th and 13th at NaMLab. Well-known researchers such as Prof. S. Salahuddin from UC Berkeley, Prof. A. Gruverman from U. Nebraska, Prof. M. H. Park from Busan National University and Prof. B. Noheda from U. Groningen contributed to the events with presentations. The Novel High-k Application Workshop was followed on September 14th and 15th by a workshop on various process technologies, jointly organized by Oxford Instruments and NaMLab. The Novel High-k Application Workshop in 2023 on May 10th and 11th ended with a record number of participants. With this series of annual workshops organized by Dr. Schröder, NaMLab continued to provide a platform for application-oriented scientists to exchange ideas and discuss the latest experimental results.

Summer School contributions 2022/2023

After the long COVID-19 pandemic crisis, several summer schools opened their doors and took place again. NaMLab speakers contributed e.g. to the IEEE UFFC Ferroelectric School Summer School 2022 in Lyon, France, and 2023 in Xian, China, as well as to the Energy efficient embedded artificial intelligence (E3AI) Summer School 2023 in Bordeaux, France. This format helps young scientists to access the latest results in their field and to establish closer contacts with experienced researchers.

NaMLab In The Media



Various press articles about research at NaMLab

Contact: Prof. Dr.-Ing. Thomas Mikolajick

Publication List 2022/2023

Journal Papers 2022-2023

J1	H. Zhou, J. Ocker, S. Müller, M. Pesic, and T. Mikolajick, “Polarization Switching and Charge Trapping in HfO2-Based Ferroelectric Transistors,” IEEE Electron Device Letters, vol. 44, no. 11, pp. 1903–1906, Nov. 2023, doi: 10.1109/LED.2023.3318294.
J2	B. Xu et al., “Strain as a Global Factor in Stabilizing the Ferroelectric Properties of ZrO2,” Advanced Functional Materials, vol. n/a, no. n/a, p. 2311825, 2023, doi: 10.1002/adfm.202311825.
J3	B. Xu et al., “Strain as a Global Factor in Stabilizing the Ferroelectric Properties of ZrO2,” Advanced Functional Materials, vol. n/a, no. n/a, p. 2311825, 2023, doi: 10.1002/adfm.202311825.
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C28	R. Alcala et al., "BEOL Integrated Ferroelectric HfO2 based Capacitors for FeRAM: Extrapolation of Reliability Performance to Use Conditions," in 2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Mar. 2022, pp. 67–69. doi: 10.1109/EDTM53872.2022.9798048.

Conference Proceedings 2022-2023

C29	J. Trommer et al., “Design Enablement Flow for Circuits with Inherent Obfuscation Based on Reconfigurable Transistors.” In 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE), 1–6. Antwerp, Belgium: IEEE, 2023. https://doi.org/10.23919/DATE56975.2023.10136918.
C30	S. Slesazeck et al., “Hyper Dimensional Computing with Ferroelectric Tunneling Junctions.” In Proceedings of the 18th ACM International Symposium on Nanoscale Architectures, 1–2. Dresden Germany: ACM, 2023. https://doi.org/10.1145/3611315.3633239.

Monographs (Book Chapters) 2022-2023

M1	S. Slesazeck, H. Mulaosmanovic, M. Hoffmann, U. Schroeder, T. Mikolajick, and B. Max, “Chapter 8 - MOx in ferroelectric memories,” in Metal Oxides for Non-volatile Memory, P. Dimitrakis, I. Valov, and S. Tappertzhofen, Eds., in Metal Oxides. , Elsevier, 2022, pp. 245–279. doi: 10.1016/B978-0-12-814629-3.00008-8.
M2	Rai, S. Rai et al., “END-TRUE: Emerging Nanotechnology-Based Double-Throughput True Random Number Generator.” In VLSI-SoC: Technology Advancement on SoC Design, 661:175–203. IFIP Advances in Information and Communication Technology. Cham: Springer Nature Switzerland, 2022. https://doi.org/10.1007/978-3-031-16818-5_9.

Invited Talks 2022-2023

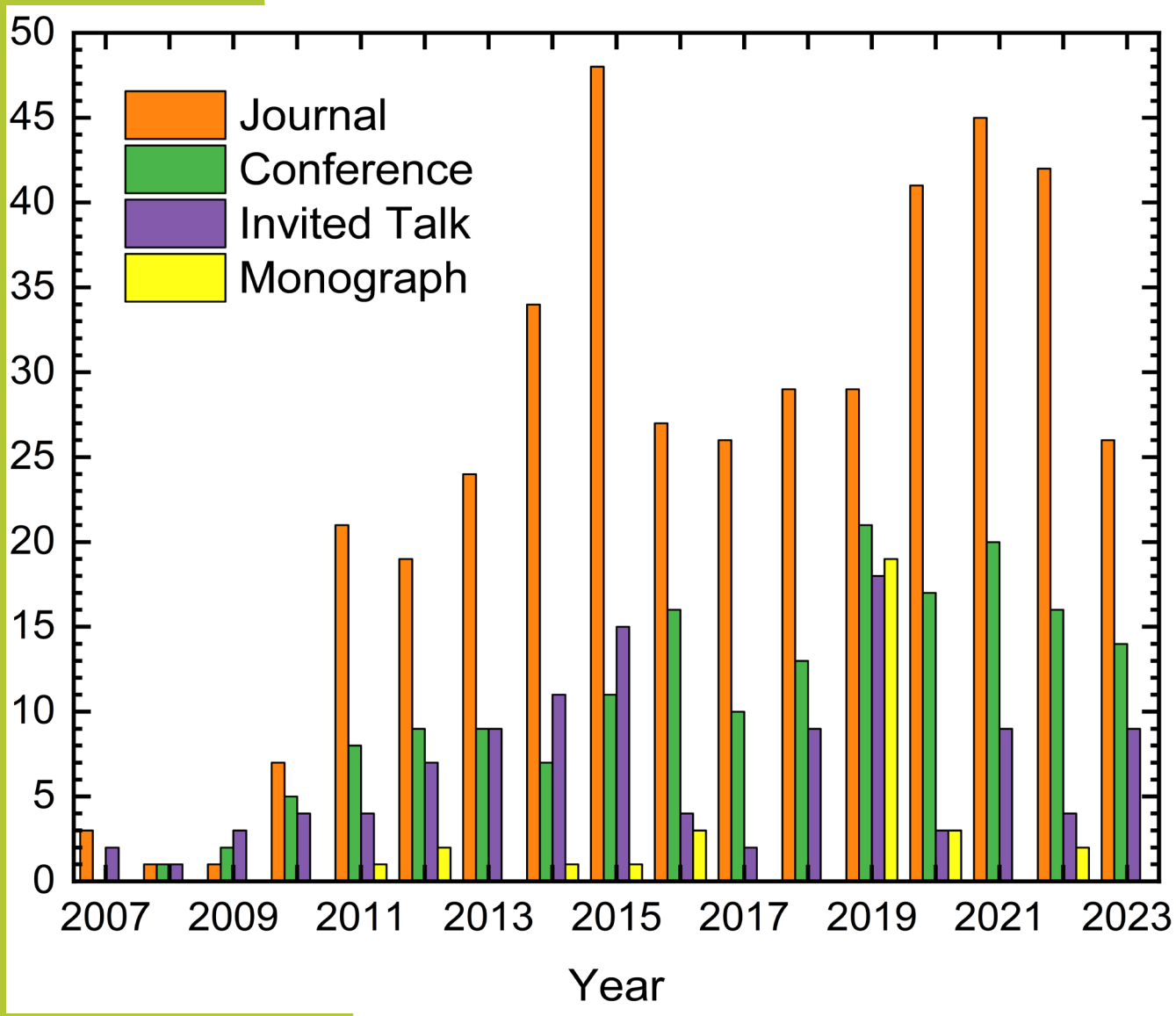
I1	Uwe Schroeder, “Ferroelectric Hafnium Oxide for non-volatile memory and neuromorphic applications”, IEEE Ferro School 2022 Lyon, 20-24 June 2022.
I2	Jens Trommer, “Insights into the Temperature Dependent Switching Behaviour of Three-Gated Reconfigurable FETs”, EMRS Fall Symposium, Warsaw, Poland, 19-22 September 2022.
I3	Uwe Schroeder, “Doped ferroelectric HfO2: from Material to Devices”, ISIT Kiel, 2022.
I4	Uwe Schroeder, “BEOL Ferroelectric HfO2 Capacitors for FeRAM: from single devices to memory arrays”, NVMTS Stanford, 7-9 December 2022.
I5	Uwe Schroeder, “Ferroelectric Hafnium/Zirconium Oxide: From Memory Devices to Emerging Applications”, Semicon, Korea, 1-3 February 2023.
I6	Uwe Schroeder, Cheol Seong Hwang ,“From fundamentals to capacitor applications for doped HfO2-based ferroelectrics”, IMF, Tel Aviv, 26-30 March 2023.
I7	Suzanne Lancaster, ”Characterisation and device integration of ferroelectric hafnia for neuromorphic applications”, CMD30/FisMat 2023 – General Conference of the Condensed Matter Division of the European Physical Society, Milan, 4-8 September 2023.
I8	Uwe Schroeder, “BEOL Ferroelectric HfO2 Capacitors for FeRAM: from Single Devices to Memory Arrays”, Seoul National University, Korea, 2023
I9	Uwe Schroeder, “Atomic Layer Processing of Hafnia-Zirconia Ferroelectrics”, EFDS, ALD for Industry, Dresden, 2023.
I10	Uwe Schroeder, “Doped HfO2-ferroelectrics: From Fundamentals to Pyroelectric Properties” The University of Chicago, USA, 2023.
I11	Uwe Schroeder, “Ferroelectric Hafnium Oxide for non-volatile memory and neuromorphic applications”, Ferro School Xi‘an, China, 2023.
I12	Bohan Xu, Uwe Schroeder, “Strain as a Key Factor for Stabilizing Ferroelectric Properties in Hafnium and Zirconium Oxide” Penn State, USA, 2023.
I13	Uwe Schroeder, “Phases and phase transitions in ferroelectric doped HfO2”, MRM Japan, Kyoto, 2023

Education

PhD theses 2022-2023

P1	Anthony Calzolaro, “Fabrication and Characterization of AlGaN/GaN MIS HEMTs for High Power Applications”, 2022.
P2	Melanie Herzig, “Optimization of NbOx based threshold switches for oscillator based applications”, 2022.
P3	Monica Materano, “Optimization of performance and reliability of HZO based capacitors for ferroelectric memory applications”, 2022.

Publication Statistics



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