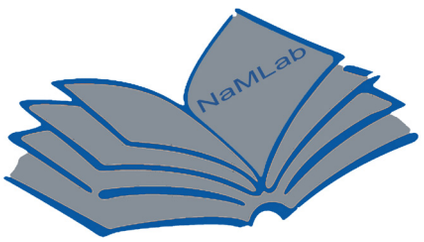
namlab

a tu dresden company

Two-Year Report 2020.2021

Highlights 2020/2021

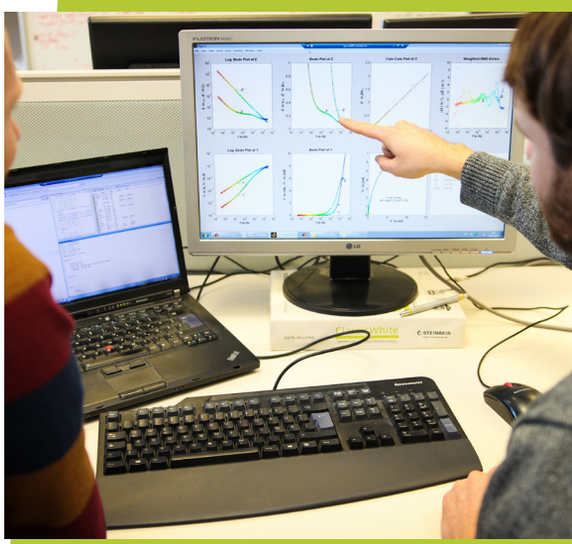
Employees 42	PhD Students 16



Publications 123	Citations >8500

Patent applications/ Patents 9/5	Research Projects 24

Content



Prof. Dr.-Ing. Thomas Mikolajick

Preface

NaMLab was founded in 2006 as a public private partnership between Qimonda Dresden GmbH and TU Dresden. In the first year, NaMLab started as a research organization with 10 employees focused on material research for future memory devices. The company steadily expanded and today, NaMLab serves a growing list of world-wide partners. NaMLab's research is contributing to the main challenges for our future society with respect to climate change, digitalization and mobility by placing sustainable, secure and intelligent electronic solutions into the core focus. With respect to the technical areas those solutions can be divided into three main activities:

- Dielectrics for Semiconductor Devices,
- Reconfigurable Devices and
- Energy Efficiency Devices

This sixth bi-annual report covers the NaMLab activities in the two year period 2020 and 2021. The timeframe was strongly influenced by the Sars-Cov2 pandemic. Especially a research organization working mainly experimentally is affected by this boundary conditions. The team pulled together and met the challenge with great success. The institute continued its path as a world leading organization in the field of material research for future electron devices. The level of international attention has again increased.

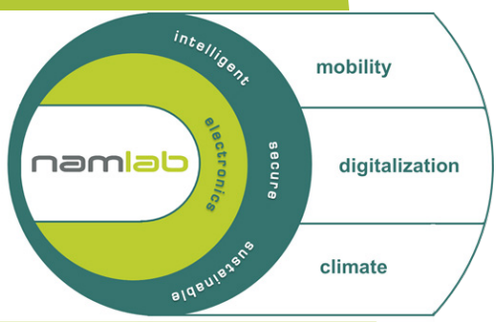
NaMLab's research in the field of dielectrics is focused on fluorite-structure ferroelectric materials, such as hafnium oxide, and their application in capacitors. The understanding of the main factors that control ferroelectricity in hafnium oxide, as well as the understanding of the degradation mechanism of such ferroelectric materials was a focus point of the research. As one highlight, the optimized material stacks have been integrated into two 1T-1C FeRAM demonstrators successfully. This shows the strong link of between the research on dielectrics and device oriented topics NaMLab has achieved.

All three reconfigurable device concepts explored at NaMLab are currently under consideration for applications in both intelligent self-learning electronics as well as electronics with a higher inherent security.

In a reconfigurable field effect transistor (RFET), the polarity of a field effect device can be controlled by applying a gate voltage to a dedicated programming gate. In the reporting period, the team, together with an industrial partner, was able to demonstrate a first RFET device integrated into a state of the art CMOS technology. Moreover, this research field was significantly extended towards applications in hardware security.

The second topic in reconfigurable devices is field effect transistors based on ferroelectric hafnium oxide. Together with partners from Fraunhofer IPMS-CNT and GLOBALFOUNDRIES, NaMLab is pushing this concept since 2009.

On this topic in the reporting period, NaMLab continued by working with GLOBALFOUNDRIES and the NaMLab Spin-Off Ferroelectric Memory GmbH on developing the embedded FeFET technology at GLOBALFOUNDRIES. Applications of ferroelectric hafnium oxide beyond semiconductor memories like neuromorphic computing and



The research activities of NaMLab are connected to the main societal challenges: mobility, digitalization and climate change by focusing on intelligent, secure and sustainable electronic devices.

Dielectric Materials

Capacitor Dielectrics
Flurite Structure Ferroelecrics

Reconfigurable Devices

Reconfigurable Nanowire Devices
Ferroelectric Devices
Resistive Switching Devices

Energy Efficiency Devices

GaN Devices
Dielectrics for Solar Cells
Anodes for Li-Ion Batteries

Overview of research activities at NaMLab

memory-in logic devices were a focus point. Besides FeFET based devices also ferroelectric tunneling junctions (FTJ) have become more important to realize artificial synapses.

The third major reconfigurable device concept explored is resistive switching. Here, new aspects of the threshold switching in niobium oxide have been explored that enable circuit demonstrators for new computing paradigms. As an example, the possibilities to use coupled oscillators to solve the very important graph coloring problem was explored together with the group of Prof. Tetzlaff at TU Dresden. Moreover, new projects to realize analog resistive switching as well as memcapacitance have been started in the reporting period.

The field of energy efficiency devices has three key topics, namely solar cells, batteries and GaN materials and devices. All three research activities aim on providing sustainable electronic solutions. The focus of the field of solar cells was the development of conducting passivation layers building upon NaMLab's expertise in dielectric materials. Results showing the feasibility of the different components: conductivity and surface passivation have been successfully demonstrated. Based on the know-how in bottom-up nanowire fabrication, anodes for lithium-ion batteries were processed. In this reporting period a method to characterize the stability of silicon anodes using in-situ Raman spectroscopy was extended to characterize different silicon based anode configurations supplied by partners.

In the field of gallium nitride materials and devices at the outpost in Freiberg, together with its industrial partner NaMLab was able to further enhance the quality and reproducibility of crack-free doped HVPE GaN crystals. At the same time, in the MBE activities high quality films reflecting the understanding of the emergence and the impact of remaining impurities was further improved. In the field of GaN devices, first fully vertical devices have been produced and the optimization of these devices is ongoing. Moreover, a new Tantalum based gold free contact scheme for HEMT devices was developed and the stability of Al_2O_3 integrated as a gate dielectric into MISHEMT devices was improved.

In summary, despite the complicated boundary conditions induced by the Sars_Cov2 pandemic, NaMLab further strengthen its position in the core topics, contributing to the grand challenges of our modern society in the reporting period. This is documented in the increasing number of partnerships with local and international industrial and research partners. Another impressive increase of citations of NaMLab's scientific publications as well as a large number of invitations to leading scientific conferences like IRPS, ISAF, EDTM etc. document the high international visibility NaMLab has now achieved and maintained. The NaMLab team will built on the strong results accomplished in this reporting period and further extend its efforts to continuously contribute to shape the exciting and challenging world of micro- and nanoelectronics.

Prof. Dr.-Ing. Thomas Mikolajick

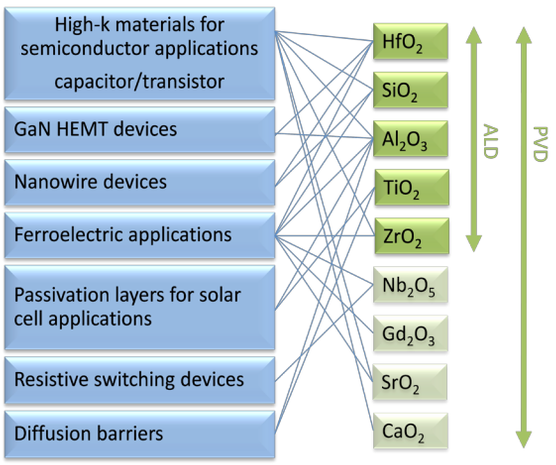
NaMLab Team

Dielectric Materials

Overview Dielectrics

Materials with high dielectric constant (high-k materials) play an increasingly important role in nano-electronic devices. For example, the charge is stored in capacitors with a dielectric insulation layer in conventional semiconductors. In order to maintain the storage capacity of capacitors, new dielectric materials with higher dielectric constants have to be introduced for devices with smaller areas. Similar dielectric materials are needed for the next generation of high-performance transistors for processors and logic products. A variety of research projects in the nano-scale regime are ongoing to understand material properties with respect to leakage mechanisms, performance, speed, and reliability.

The schematic below depicts five central material systems (Al_2O_3, HfO_2, ZrO_2, TiO_2, and SiO_2) researched for different dielectric applications. Accordingly, the detailed understanding of the structural and electrical properties gained for one device application can be used as a fundamental knowledge base for future new devices. The impact of process conditions on the device performance can be correlated. Especially optimizing material properties like density, dielectric, piezoelectric, ferroelectric, and optical properties or charges and traps is essential for various device applications.



NaMLab also screens and characterizes further candidate materials like e.g. Nb_2O_5, SrO_2, and $CaTiO_3$ for novel device applications. Additional new dielectrics will follow. Materials are deposited by molecular beam deposition (MBD), atomic layer deposition (ALD), chemical vapor deposition (CVD), and physical vapor deposition (PVD) as shown in above drawing, Research at NaMLab covers a wide range of applications from dielectrics for nanowire transistors (Fig. 1), GaN HEMT devices (Fig. 2), capacitors to structures (Fig. 3).

Contact: Dr. Uwe Schroeder

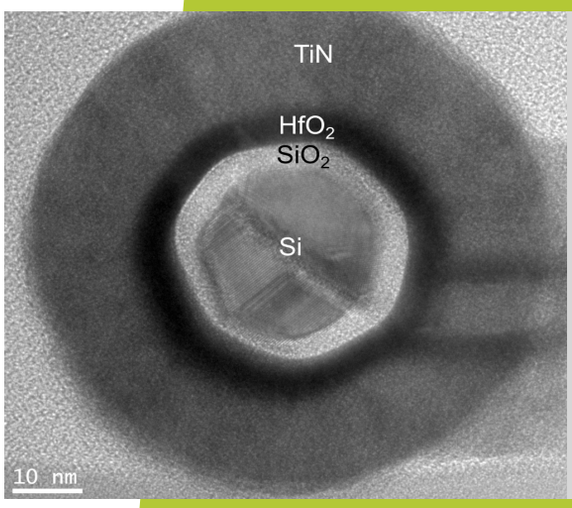


Fig. 1: ALD based dielectric materials as gate dielectric in nanowire and ferroelectric field effect transistors.

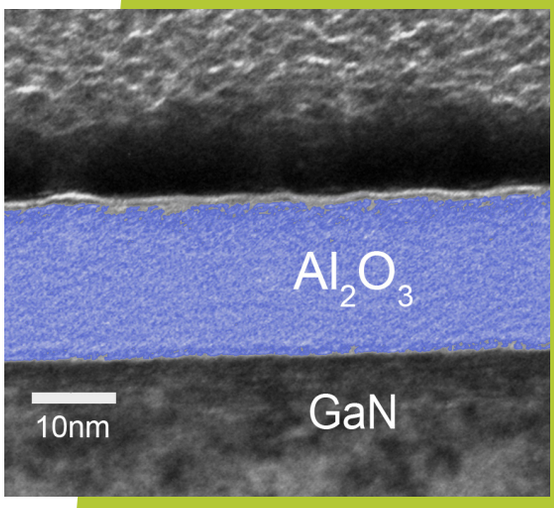


Fig. 2: Deposition of ALD Al_2O_3 dielectrics within a GaN HEMT device.

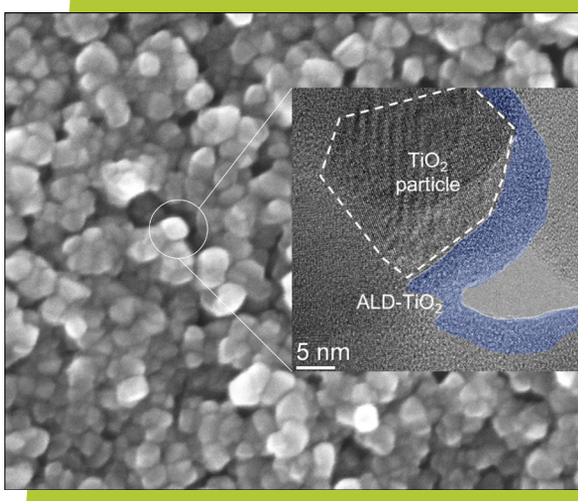


Fig.3: Deposition of ALD TiO_2 dielectric on a porous electrode with high surface area.

Hafnium Oxide Based Ferroelectric Materials

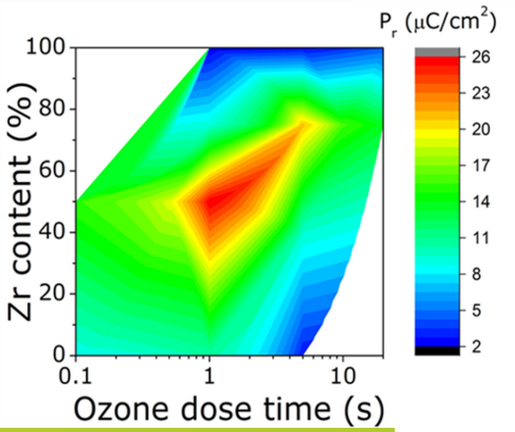


Fig. 1: Remanent polarization values for for a 10 nm thick HfZrO thin film capacitor with different HfO_2/ZrO_2 ratio and ozone dose time (oxygen vacancy content).

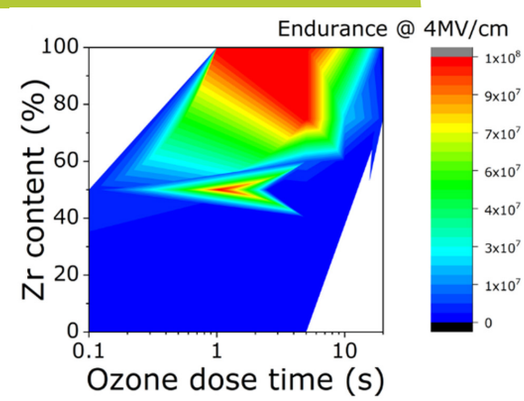


Fig. 2: Field cycling endurance for a 10 nm thick HfZrO thin film capacitor with different HfO_2/ZrO_2 ratio and oxygen vacancy content.

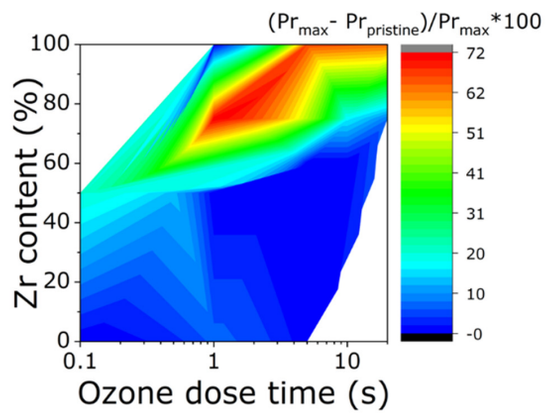


Fig. 3: Wake-up for a 10 nm thick HfZrO thin film capacitor with different HfO_2/ZrO_2 ratio and oxygen vacancy content.

During the last two years, the main focus of the development of ferroelectric HfO_2 based materials is the detailed understanding of the ferroelectric properties in thin doped HfO_2 layers. A variety of dopants materials (Si, Al, Ge, Y, Gd, La, and Sr) were studied in addition to mixed $Hf_{1-x}Zr_xO_2$ layers. Deposition techniques included atomic layer deposition and physical vapor deposition. The ferroelectric orthorhombic Pca21 phase of HfO_2 is formed when the material is crystallized with a certain dopant or oxygen concentration at the phase boundary between the monoclinic and the tetragonal/cubic phase and is enhanced through mechanical confinement. Scanning transmission electron microscopy and electron diffraction methods confirmed the structure. Continuous research aims to understand the root cause of this previously unknown phase. In particular, the effect of the interplay between the influence of different dopants or HfO_2/ZrO_2 composition ratio and the amount of oxygen vacancies as introduced by different O_3 dose times during film deposition on phase formation is under investigation. Both parameters impact thermal stability and film reliability (Figure 1-3). Based on these results, significant improvements in the film performance could be achieved. In addition, the surface and interface energy of grains in the film, together with residual stress generated during growth and crystallization annealing, can be critical parameters. Ab initio simulations by partners at the Munich UAS confirmed the influence of the factors mentioned above on the phase stability of ferroelectric HfO_2 and proposed a qualitative model.

The polarization hysteresis for all dopants showed a maximum remanent polarization value between 15-40 µC/cm², depending on the dopant material. The highest values were obtained for lanthanum doped HfO_2 with TiN electrodes. Piezo-response force microscopy (Oak Ridge Nat. Laboratory/Univ. Nebraska) in conjunction with transmission electron microscopy (North Carolina State University) measurements revealed domains within single grains with a diameter of ~20-30 nm for 10 nm thick films. The polycrystalline structure of the films caused a varying polarization orientation within the layer. The size distribution of the grains follows a Poisson distribution resulting in a grain size-dependent coercive field and Curie temperature.

Future studies will focus on the structural basis of the ferroelectric properties, their impact on the ferroelectric switching behavior, and how device cycling performance can be improved.

Cooperation: Fraunhofer IPMS-CNT, Dresden (Germany), RWTH Aachen (Germany), UAS Munich (Germany), GLOBALFOUNDRIES Dresden (Germany), IMEC (Belgium), Oak Ridge National Labs (USA), Dalin University (China), North Carolina State University Raleigh (USA), Tokyo Institute of Technology (Japan)

Publications: J1, J7, J8, J11, J17, J18, J19, J20, J24, J25, J33, J37, J38, J43, J45, J58, J59, J60, J62, J63, J64, J67, J68, J69, J70, J71 J76, J77, J78, J83, C6, C7, C9, C10, C11, C23, C27, I2-I10

Contact: Dr. Uwe Schroeder

Hafnium Oxide Based Pyro-electric Materials

The main focus of the work is on a detailed understanding of the pyroelectric properties (PE) in thin doped HfO_2 layers. Pyroelectric properties were characterized for various doped HfO_2 and $Hf_{0.5}Zr_{0.5}O_2$ films with different thicknesses.

A survey of the pyroelectric behavior was undertaken for a wide varie-ty of dopants incorporated into HfO_2 including Al, Gd, Sr, and La as well as the $Hf_{0.5}Zr_{0.5}O_2$ composition. In addition to understanding the effect of different dopants, a detailed investigation of the pyroelectric dependence on the Si-concentration in Si-doped HfO_2 thin films was carried out to evaluate the influence of the doping concentration on the pyroelectric performance. The Sharp-Garn method detects the current response upon a sinusoidal temperature stimulation was used to accurately determine the pyroelectric coefficients in ferroe-lectric films. Infrared sensing applications for example require a linear and reversible transduction of temperature into electrical charge (Fig. 1).

The pyroelectric coefficients in Si-doped HfO_2 films were stable over a 0 – 170 °C temperature range which is very promising for sensing applications using the pyroelectric effect. Of all the different types of HfO_2-based thin film capacitors investigated by NaMLab so far, $Hf_{0.5}Zr_{0.5}O_2$ exhibited the largest remanent polarization and the largest pyroelectric coefficient of 70 $\mu C\ K^{-1}\ m^{-2}$.

To further investigate the excellent pyroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ thin films, both the poling and film thickness dependence was investigated. The pyroelectric coefficient in $Hf_{0.5}Zr_{0.5}O_2$ was found to exhibit an electric field poling dependence due to the different polarized states of the ferroelectric films (Fig. 2). With strong pulsed poling fields, the pyroelectric coefficient saturates by maximizing the remanent polarization induced in the ferroelectric films. The role of film thickness was determined by varying $Hf_{0.5}Zr_{0.5}O_2$ films from 10 – 30 nm in thickness. The highest pyroelectric coefficients and best figures of merit were obtained in 10 – 15 nm $Hf_{0.5}Zr_{0.5}O_2$ thin films annealed at 450 °C (Fig. 3), whereas the pyroelectric performance in thicker films and higher annealing temperatures was degraded due to the formation of the monoclinic phase and low-k interfacial layers. Through the Landau-Devonshire Gibbs energy equation for ferroelectrics, a relationship between the dielectric, ferroelectric, and pyroelectric properties was established in all types of HfO_2-based thin films by the Curie constant.

Upcoming studies will investigate the pyroelectric effect with new structures and operating conditions for sensing and energy harvesting applications.

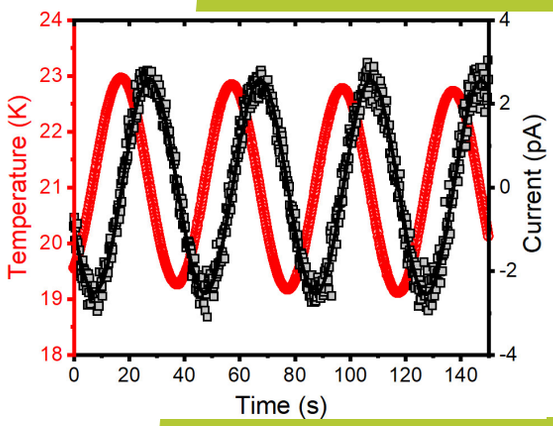


Fig.1: Sharp-Garn pyro-electric measurement performed on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$.

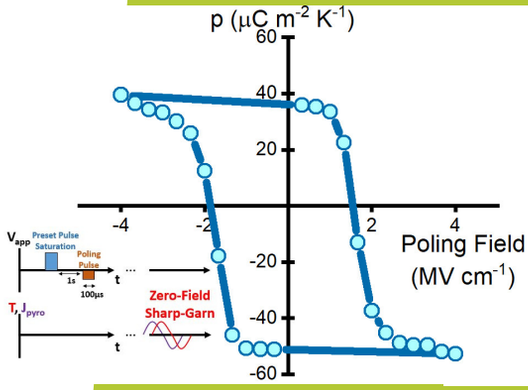


Fig. 2: Poling field dependence of the pyroelectric coefficient in $Hf_{0.5}Zr_{0.5}O_2$ thin film capacitors.

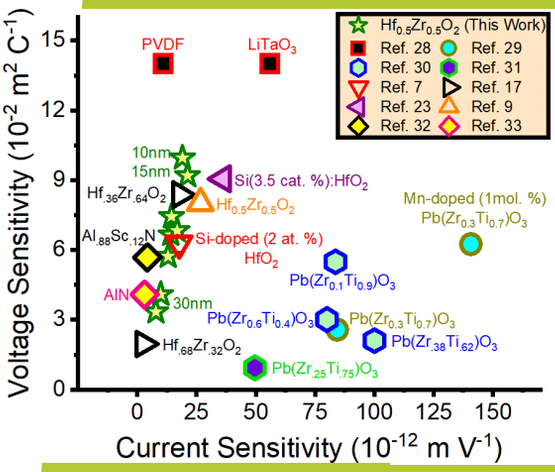


Fig. 3: Voltage sensitivity and current sensitivity figures of merit of $Hf_{0.5}Zr_{0.5}O_2$ thin films of different thicknesses for infrared sensor material benchmarking.

Cooperation: RWTH Aachen (Germany), Hochschule München (Germany), Oak Ridge National Labs (USA), TU Bergakademie Freiberg (Germany)
Publications: J16, J48, J61

Contact: Patrick D. Lomenzo

Reconfigurable Devices

Capacitor Based Ferroelectric Memory

During the last two years, the main focus was on transferring the metal-ferroelectric-metal capacitor stack from the lab, having a diameter of about 100 µm, to memory arrays with 100-1000 times smaller feature sizes. Concurrently, the optimization of the film and film stack properties to improve the reliability of the ferroelectric capacitor according to industry specifications was addressed. The goal is to develop back-end-of-line (BEOL) compatible capacitors with a maximum thermal budget of 500 °C or below. The ferroelectric material of choice is an atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$. The activity was conducted with industrial partners, including LETI and ST, within the European project '3eFerro' and Sony. 16 and 64 kbit sized memory arrays with $Hf_{0.5}Zr_{0.5}O_2$ based capacitors were realized with a high yield on 200 mm hardware.

The polarization hysteresis of $Hf_{0.5}Zr_{0.5}O_2$ based capacitors showed a maximum remanent polarization of about 25 µC/cm². In addition, the influence of lanthanum- and aluminum-oxide interface layers with $Hf_{0.5}Zr_{0.5}O_2$ on the field cycling behavior was examined, and a stable cycling behavior up to 10^{10} cycles was achieved (Figure 1). Wake-up, internal bias fields, fatigue, imprint, and retention effects in $Hf_{0.5}Zr_{0.5}O_2$ are generally dominated by charge trapping effects at defects mainly located at the $Hf_{0.5}Zr_{0.5}O_2$/electrode interface. Furthermore, depolarization effects can be caused by nonpolar phases. Structural changes associated with field-induced phase transitions were highly suppressed with less than 1 % lattice volume changes in synchrotron-based diffraction measurements. The length of the oxidant pulse within the atomic layer deposition process plays a significant role in the phase formation and the reliability properties of the capacitor structure (Figure 2). The duration of the ALD oxidant pulse strongly impacted the ferroelectric properties and device reliability, which was then used to optimize ALD processing. Due to the resulting voltage-time trade-off to achieve > 90% domain switching after 10 ns, a voltage of about 2.5 V has to be applied to 10 nm thick films.

Both development partners introduced the $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric material into their memory arrays and reached a field cycling endurance > 10^{11} for sub-1 µm capacitor structures (Figure 3). Sense amplifiers read-out stored polarization states and good read voltage margin with a 2.5 V operation voltage and confirmed an operating speed of about 10 ns for 16 and 64 kbit memory arrays.

Future studies will focus on further understanding the structural basis of the ferroelectric properties and their impact on the ferroelectric switching behavior to improve cycling performance for introduction into larger memory arrays.

Cooperation: CEA Saclay / CEA-LETI (France), ST Microelectronics (France), National Institute of Materials Physics (Romania), EPFL (Switzerland), Ecole Centrale De Lyon (France), NCSR „DEMOKRITOS" (Greece), Forschungszentrum Jülich (Germany), Sony (Japan)

Publications: J25, J33, J49, J63, J67, J75, C3, C14, C22, C27, C30, C31

Contact: Dr. Uwe Schroeder

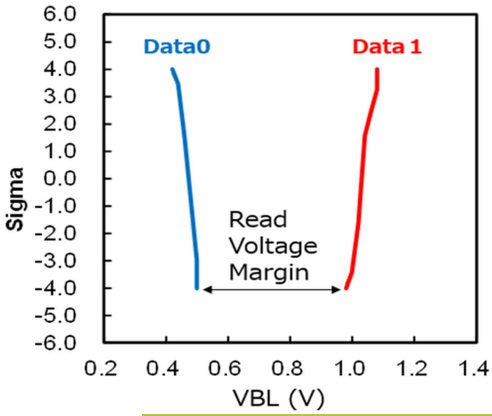


Fig. 1: Read voltage margin for array capacitors with ~10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ (VLSI 2020).

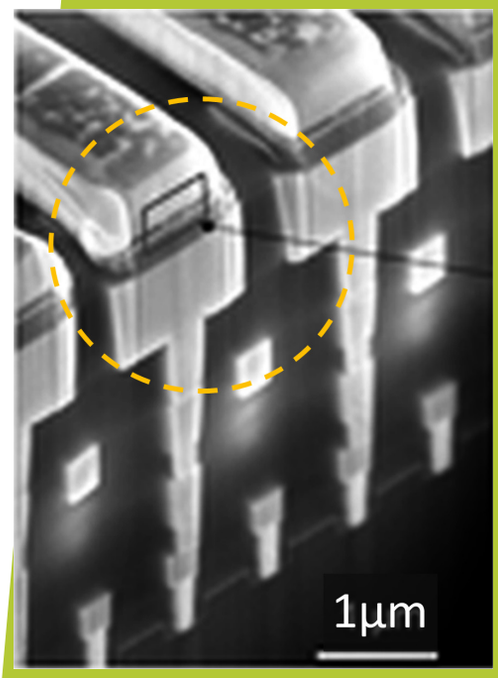


Fig. 2: SEM cross-section of 10 nm thick HfZrO films within a 16kbit capacitor-based memory array fabricated within the 3eFerro EU project with partners LETI/ST (VLSI 2020).

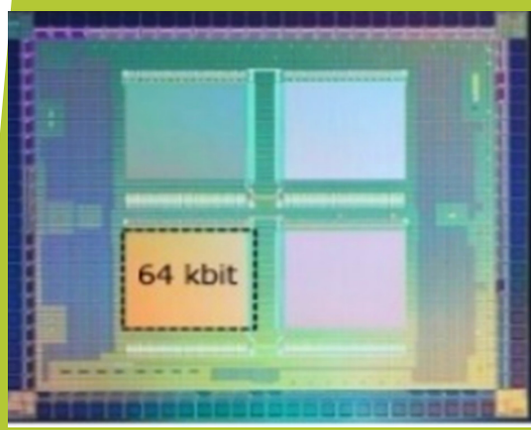


Fig. 3: Optical microscope image of 64kbit capacitor-based memory array fabricated with partner Sony (VLSI 2020).

FeFET Based Ferroelectric Memory

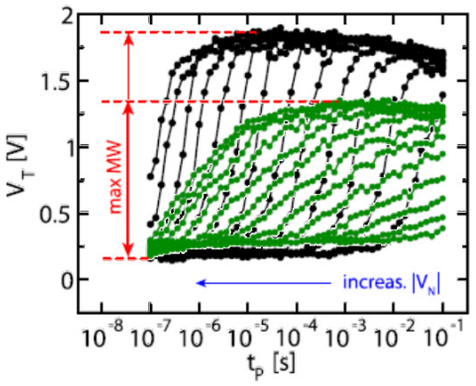


Fig. 1: Switching kinetics measurements for 28nm FeFETs with different Si-concentration in the ferroelectric Si-doped HfO_2.

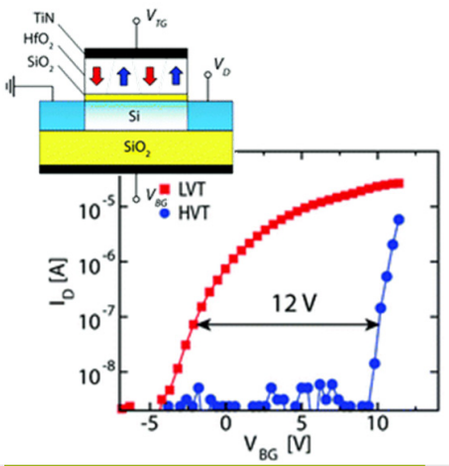


Fig. 2: Measured I_DV_{BG} characteristic of n-FeFET devices based on 22nm FDX technology. The adoption of the back-gate allows device operation with a record-high memory window.

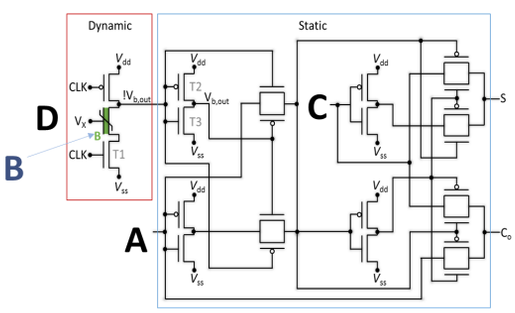


Fig. 3: Circuit diagram of a novel mixed static/dynamic full adder where one summand is stored non-volatile as polarization state of the FeFET.

HfO_2-based ferroelectric memories are long-term contenders for ultra-fast, low-power and non-volatile memory technologies. The electric polarization reversal in ferroelectric thin films is adopted in different memory devices. While the write operation is always conducted by applying an electric field in either polarity to the ferroelectric film, the read operation distinguishes three main concepts. In the FeRAM mode, the displacement current of a ferroelectric capacitor (FeCAP) is directly measured during polarization reversal, leading to a destructive read operation. In contrast, in the ferroelectric tunneling junction (FTJ) the polarization state dependent leakage current is measured and is indicative for the stored data. Finally, in ferroelectric field-effect transistors (FeFET) the information is stored as a polarization state of the gate dielectric and can be read non-destructively as a shift of the threshold voltage of the transistor. In collaboration with GLOBALFOUNDRIES FeFET devices were successfully implemented in a 28nm gate-first super low power (28SLP) and 22nm FDX CMOS technology platforms using only two additional structural masks. In our work we concentrate on the electrical characterization, modeling of the FeFET and their adoption in memory arrays or novel hardware accelerator circuits for the implementation of AI-algorithms. Fig. 1 shows the measurement results of a switching kinetics measurement that was performed on FeFET devices manufactured in 28nm SLP technology. Two different process variants were investigated. The diagram depicts the evolution of the threshold voltage when applying erase pulses with increasing amplitude and pulse width. With our results we aim at further optimizing the FeFET technology at GLOBALFOUNDRIES and to support our start-up company FMC (Ferroelectric Memory Com-pany, www.ferroelectric-memory.com) targeting at the commercialization of the FeFET-based memory, which was developed in Saxony during the recent years. Fig. 2 reports the measured I_DV_{BG} characteristic of a FeFET being manufactured in 22nm FDX technology. The voltage sweep at the back-gate instead of the front-gate allows the operation of the device with a record-high memory window of up to 12 V. The simultaneous adoption of front- and back-gate voltages to alter the operation point of the devices opens new and interesting opportunities for circuit designs. Besides device characterization and modeling we further engage in the development of memory cells and circuit building blocks for novel computing paradigms such as compute-in-memory or neuromorphic concepts. Fig. 3 shows the circuit diagram of our recently proposed static-dynamic full-adder that allows to store one summand locally as polarization state of the FeFET. The circuit is used to realize a multi-layer perceptron and a demonstration of image recognition algorithms.

Cooperation: GlobalFoundries (Germany/USA), Fraunhofer IPMS-CNT, FMC, University of Lyon

Publications: J4, J25, J26, J27, J28, J29, J30, J33, J46, J56, J67, J72, J73, J74, C1, C10, C12, C13, C16, C17, C25, C27, C28, M1, M2, P2

Contact: Dr. Stefan Slesazeck

Ferroelectrics For Beyond Von Neumann Computing

The increasing amount of data being processed in today's electronic devices for classification tasks in image and audio recognition, autonomous driving, smart sensors signal processing or machine learning, requires a transition from the conventional compute centric paradigm to a more data centric paradigm. In the classical von Neumann architecture, the data is transferred between computing and memory units via a bus system with limited bandwidth, giving rise to the well-known von Neumann bottleneck. In order to bridge the existing gap between memory and logic units, the concept of physical separation between computing and memory unit has to be repealed.

Ferroelectric Tunnel Junction (FTJ) devices can be applied as synaptic weighting elements in neuromorphic processors. These architectures use artificial neurons and synapses to emulate biological primitives underlying learning. In particular, the synapses act as both storage and computing element. Indeed, their role is to facilitate or inhibit the connection between neurons by changing their weight. In case of FTJs devices, the change of weight is mapped into a change of the device conductance.

In order to use FTJ devices for applications in beyond-von Neumann computing, their properties should be further improved, for example increasing the tunneling current and the tunneling electroresistance ratio. On a device level, this requires a better understanding of the influence of charge trapping on polarization switching, thorough characterization for on-chip operation, as well as back-end-of-line (BEOL) integration. Additionally, BEOL-compatible processes can be developed to modify device behavior, such as work function engineering of the electrodes for increasing tunneling currents.

Novel devices based on spin-orbit interactions offer an alternative route to non-volatile memory devices. Skyrmions in magnetic bilayers can be used for memory-in-logic, with the additional benefit that they are topologically protected and highly robust. The integration of ferroelectric thin films with magnetic bilayers and device stacks designed for spin-orbitronics thus enables investigation into a new generation of highly efficient, low-power, non-volatile components for beyond von Neumann computing.

Cooperation: GlobalFoundries, X-FAB, IBM, IMDEA Nanociencia, CEA-Leti, CNRS Thales, UAM, University of Udine, HZB, NCSRD, IUNET, UNIMORE, University of Groningen, University of Zürich and ETH Zurich

Publications: J22, J23, J58, C20, C21, P4

Contact: Dr. Stefan Slesazeck

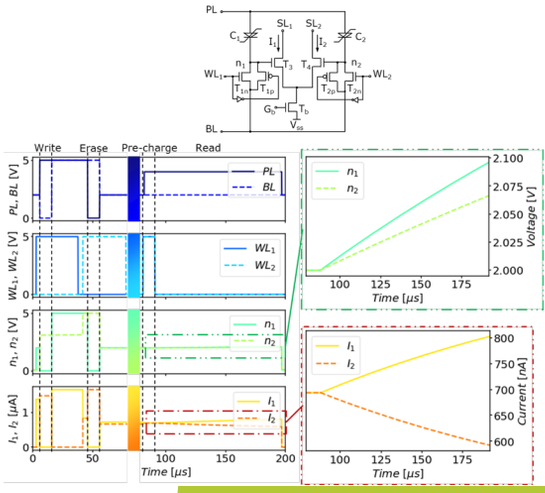


Fig. 1: Circuit schematic of a differential 2T1C cell (top) and simulation of write, pre-charge, and read operations in a differential 2T1C cell (bottom). The coloured rectangles indicate an arbitrary time span between write and pre-charge operations. Insets: zoom of n_1, n_2 voltages and I_1, I_2.

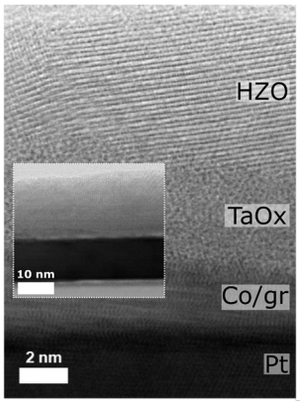


Fig. 2: High-resolution transmission electron microscopy image of polycrystalline, ferroelectric HZO film on graphene/Co/Pt stacks for the electric field control of spin-orbitronic device stacks.

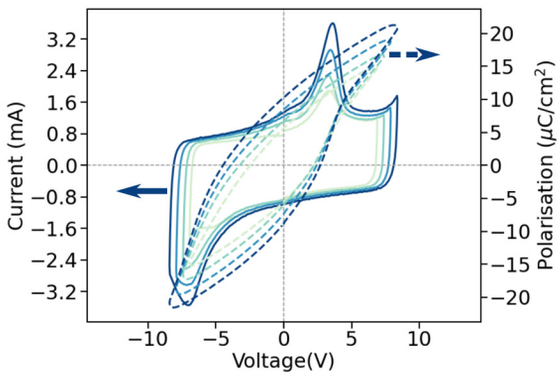


Fig. 3: Ferroelectric switching measured on HZO on graphene, demonstrating 2Pr up to 19.2 µC/cm² (bottom).

Negative Capacitance Devices

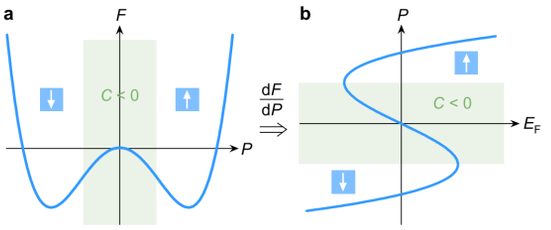


Fig. 1: a) Double-well energy landscape of a ferroelectric. b) S-shaped polarization-electric field curve showing negative capacitance.

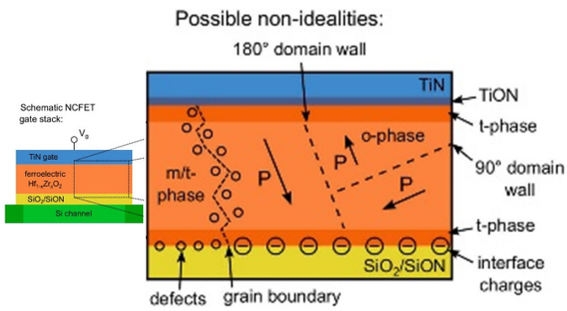


Fig. 2: Illustration of possible non-idealities in a ferroelectric-dielectric bi-layer stack that is researched for stabilization of negative differential capacitance effects.

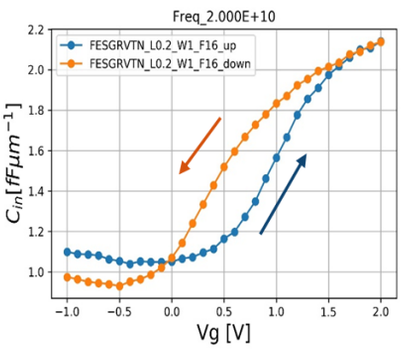


Fig. 3: Small-signal capacitance of a FeFET extracted from RF S-parameter measurements that were performed at 20GHz using dedicated RF-test structures.

Since the 1940's, phenomena in ferroelectric materials have been successfully modelled based on the Landau theory of phase transitions, which was first applied to ferroelectrics by Ginzburg and Devonshire. Phenomenological models based on this Landau–Ginzburg–Devonshire (LGD) approach have been an essential tool in understanding the basic physics of ferroelectricity. In LGD theory, a ferroelectric below its transition temperature is described by a double-well free energy landscape F as a function of the polarization P (Fig. 1a). The two degenerate energy minima define two stable spontaneous polarization states in the material, which can be reversed by the application of an electric field. By differentiating F with respect to P, one obtains the 'S'-shaped P(E), where E is the electric field in the ferroelectric (Fig. 1b). This 'S'-shape of the P(E) curve implies that in a certain region around P≈0 the ferroelectric possesses a negative differential capacitance (NC), because the capacitance C is proportional to the slope dP/dE, which is a direct consequence of the energy barrier in the double-well free energy landscape. In theory, NC can be used to increase the capacitance of a dielectric layer by adding a ferroelectric layer and as such promises the realization of power effi-cient high-performance devices and supercapacitors. NaMLab's research in this field focusses on the verification and physical understanding of the NC effects that were observed in ferroelectric HfO_2. The outcome of this work will further guide the development of ferroelectric devices tackling the trade-off between ferroelectric switching, charge-trapping and depolarization effects in ferroelectric/dielectric multi-layer stacks. Thereby, all the physical and electrical influences from electrodes, additional layers or the domain dynamics in the ferroelectric layer itself and different kinds of non-idealities are considered (Fig. 2). The work performed at NaMLab includes the fabrication, physical and electrical characterization as well as modeling of ferroelectric capacitor-based devices.

A joint project with GLOBALFOUNDRIES opens the opportunity to investigate the ferroelectric switching characteristics by means of small-signal RF-characterization using specifically designed FeFET RF-structures. Fig. 3 depicts the extracted small-signal gate capacitance of FeFETs for a double voltage sweep in the range of [-1.0V .. 2.0V]. Besides the expected shift in the threshold voltage of the erased state (blue) vs. the programmed state (orange) also a polarization-dependent capacitance change is observed under depletion condition, indicating the expected behavior for NC-induced capacitance increases.

Future work will explore potential applications of NC e.g. in energy stor-age supercapacitors. Moreover, in a joint project with IKZ Berlin we investigate epitaxially grown single-crystalline ferroelectric layers that allow eliminating some non-idealities such as the influence of grain-boundaries.

Cooperation: GlobalFoundries, IKZ Berlin

Publications: J9, J10, J51, J52, J53, C4, P3

Contact: Dr. Stefan Slesazeck

Reconfigurable FETs On A Top-Down SOI Platform

With classical scaling of CMOS transistors according to Dennard's scaling rules running out of steam, new possibilities to increase the functionality of an integrated circuit at a given footprint are becoming more and more desirable. A promising concept in this sense is, to increase the functionality of each element, while keeping the footprint the same.

The reconfigurable field-effect transistor (RFET) can provide such a feature, as it is an electronic device whose conduction mechanism can be reversibly reconfigured between n-type and p-type operation modes (Fig. 1). In its most simple form it is a four-terminal device, where two gate electrodes built on a nanoscale channel are used to independently control carrier injection via Schottky Barrier tunnelling (Fig. 2). Importantly, RFETs do not rely on chemical doping caused by impurities but rather on electrostatic doping, i.e. the generation of mobile carriers via an external potential. The RFET was conceived at NaMLab and first introduced already in 2008.

NaMLab current research focus on the improvement of its lab scale device demonstrators. Typically, silicon nanowires or nanosheets are top-down structured from SOI substrates using electron beam lithography and reactive ion etching. An omega shaped metal gate is used to increase the control over the nanowire channel. Thereby, stressor shells were successfully applied as enabler for symmetric drain-currents ensuring complementary operation of digital circuits. Various transistor geometries, channel materials, scaling trends and operation modes have been explored.

A core topic in the reporting period was the understanding and control of the thermal silicide contact formation, used to create the $NiSi_2$–Si Schottky junctions at source and drain. A controlled silicidation is needed to yield a robust technology platform with improved yield for the demonstration of circuit elements. To study the underlying kinetics and to control the reactions, we introduce local volume extensions (Fig. 3) and carried out in-situ SEM experiments. This method allows to decouple the silicide growth process from variations in the metal supply and to gain a reduced length variation if applied correctly.

Cooperation: TU Dresden -cfaed; RWTH Aachen – Prof. Knoch; Helmholtz-Zentrum Dresden-Rossendorf (HZDR), University of Cambridge – Prof. Hofmann

Publications: J6, J31, J36, J54, J55, J66, J76 J80, J82, C5, P1

Contact: Dr. Jens Trommer

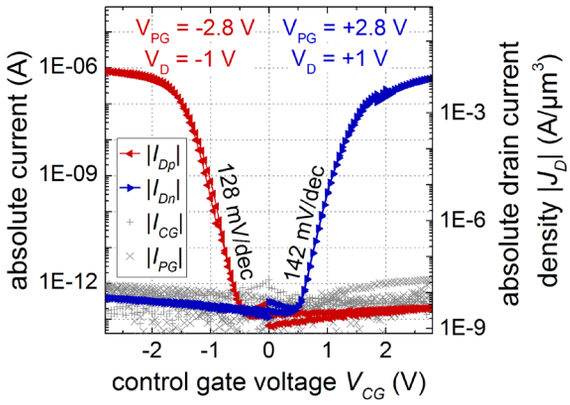


Fig. 1: Transfer characteristics of an RFET with selectable p-type (red) and n-type (blue) functionality. Device is shown in Fig. 2.

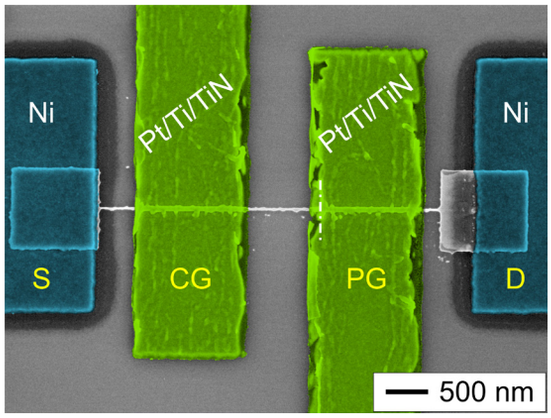


Fig. 2: Top-view SEM image of a nanowire RFET built with top-down process. The independent terminal control gate (CG), polarity gate (PG), source (S) and drain (D) are labeled. Key materials are given.

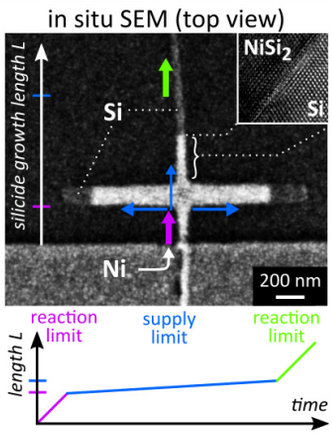


Fig. 3: In-situ SEM silicidation study. (up) Nanowire with polder structure during silicide formation event. (down) Silicide evolution over time with corresponding growth regimes, given by color.

Polymorphic Circuits for Hardware Security

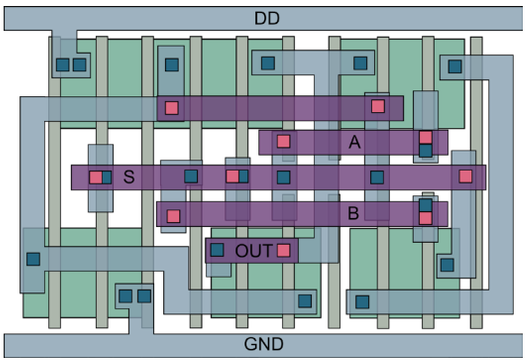


Fig. 1: Layout of a NAND/NOR cell compatible with 22 nm FDSOI design rules. The cell provides the functionality as shown in Fig. 2.

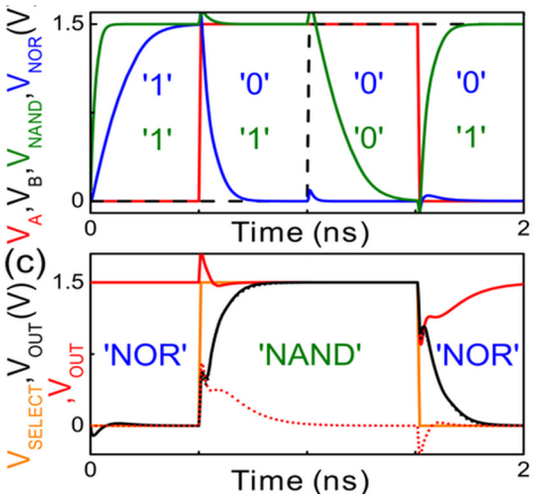


Fig. 2: Mixed-mode simulations: runtime reconfigurable opera-tion of NAND / NOR cir-cuit cell with 6 transistors. The cell always delivers full swing output.

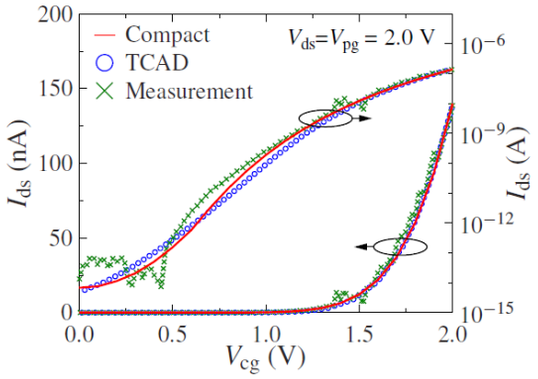


Fig. 3: Comparison of RFET n-type transfer characteristics in measu-rement, TCAD simulations and compact model, developed by one of NaMLab's partners.

The multiple operation states of reconfigurable FETs open new opportunities for logic circuit design. Mainly, two features that were previously not accessible with conventional FETs are currently being studied. First, runtime-reconfigurable logic gates can be built, providing multiple func-tionalities as programmed on the fly by volatile select signals. One basic example is given by the compact cell, which can switch from NAND to NOR operation (Fig. 1). Distinctly, those cells always operate in a complementary manner, reaching a full swing output and exhibiting the same delay for both functions (Fig. 2). The second feature is the integration of multiple gate electrodes along the channel, merging paths of series transistors within a single one, without increasing the internal resistance of the individual device. This feature can be exploited to build efficient XOR and Majority gates. Further, we recently showed the potential of such MIG-RFETs in dynamic logic gates as an elegant solution to reduce signal integrity risks such as the charge sharing effect.

RFETs gained prominence for hardware security applications, predominantly due to two features: functionality polymorphism and structural polymorphism. Just by looking at a single RFET cell, it is impossible to retrieve their underlying electrical functionality. This polymorphic nature enables new approaches on hardware security solutions, such as logic locking, camouflaging, physically unclonable functions (PUFs), or chip authentication. Considering careful gate level design solutions it is even possible to equalize the propagation delay of both the operational modes of a NAND/NOR reconfigurable logic gates, leading to near delay-invariant designs. The remaining differences in the delay traces is well hidden by the influence of process fluctuations, suggesting a high application potential in the field of securing circuits against timing side-channel attacks.

In order to bring this potential in terms of hardware security to fruition, an efficient circuit design based on RFETs requires the development of accurate models and the overall support of the electronic design automation (Fig. 3). In a first step efficient SPICE compatible models have to be developed reflecting the physics of the device, which is distinctively different than that of classical MOSFETs. These models directly use laboratory level simulations and are helpful in understanding transistor's behavior at circuit levels. Standard cell libraries have to be derived giving credit to the higher expressive capability of the RFET. Recent works have shown, that these libraries are more complex than their CMOS counterparts due to the higher expressive capabilities of RFETs.

Cooperation: TU Dresden - cfaed Prof. Kumar; TU Darmstadt – Prof. Hoffmann, Karlsruhe Institute of Technology (KIT) – Prof. Becker, Universität Bremen – Prof. Drechsler; Globalfoundries Fab 1 Dresden, TH Mittelhessen – Prof. Kloes

Publications: J32, J40, J79, C32, C34, I12

Contact: Dr. Jens Trommer

Non-Volatile NW Devices for Neuromorphic Applications

Neuromorphic computing combines specific brain-inspired integrated hard- and software that implements a behavior mimicking the biological function of a Neural Network. Artificial Neural Networks (ANNs) aim to reach the massively parallel processing ability of the human brain along with low power consumption. Typically, ANNs are three-dimensionally organized and very compact, combine storage and computation, are fault-tolerant and robust, and provide self-learning capability.

NaMLab is researching the potential application of their emerging nanowire technologies for neuronal networks. Owing to the capability to change its function by an electrical stimulus, reconfigurable transistors inherent provide this ability to adapt their functionality. This enables the replication of the plasticity of biological neuronal units such as neurons and synapses already at device level. Also the high on/off current ration of RFETs at comparatively low on-currents may pose a benefit, when it comes to the aim of mitigating power consumption in highly parallel architectures. In order to store weights in neuromorphic circuit application a combination of the reconfigurability with a non-volatile storage option is needed. Among these options our focus is on utilizing NaMLab know-how on ferroelectric materials.

Fig. 1 shows an efficient design of a non-volatile programmable XOR cell for logic-in-memory applications. Those XOR gates are also the basis of binary neuronal networks. NaMLab is currently working towards a lab-based implementation of such gates, requiring newly tailored processes and materials. Fig. 2 shows a TEM cross section of a typical SiO_2 / Hafnium-Zirconium-Oxide (HZO) / TiN stack used for non-volatile storage utilizing inherent ferroelectricity in HZO. A simple single step reactive ion etching process was developed, able to etch both TiN as well as HZO with the same parameters, but stopping precisely on SiO_2 in order to enable a subsequent self-aligned source/drain contact formation. The process will be used to integrate non-volatile storage in our future emerging nanowire devices.

A second device utilized for ANNs are junctionless transistors. Similar to RFETs these device don't rely on doping gradients and are envisioned to enable an compact neuronal network module by three-dimensional stacking. A compact model for circuit design predictions of a ferroelectric junctionless FET is shown in Fig. 3. NaMLab currently focusses on the hardware realization of these devices.

Cooperation: TU Dresden – cfaed; University of Bordeaux – Prof. Maneux; LAAS-CNRS Toulouse; University of Lyon – Prof. O'Connor; Global TCAD Solutions; EPFL Lausanne – Prof. Atienza

Publications: J21, J35, J65, C8, C24, C29, C33, I1

Contact: Dr. Jens Trommer

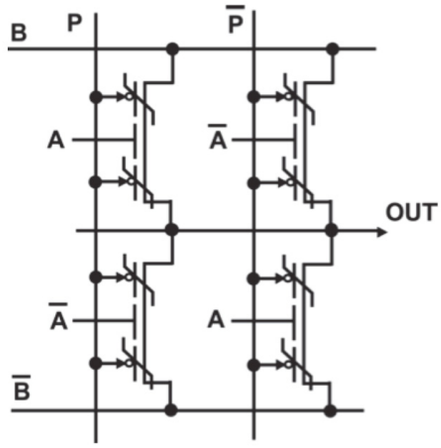


Fig. 1: A programmable XOR/ XNOR cell based on four ferroelectric RFETs with three gates each.

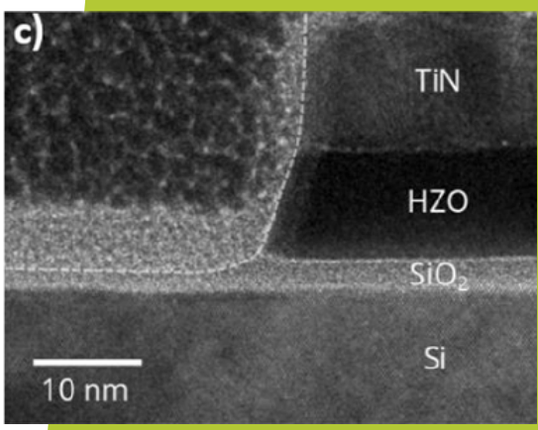


Fig. 2: TEM-image of the etch profile of a ferroelectric TiN/HZO/ SiO_2 gate stack for non-volatile storage integration.

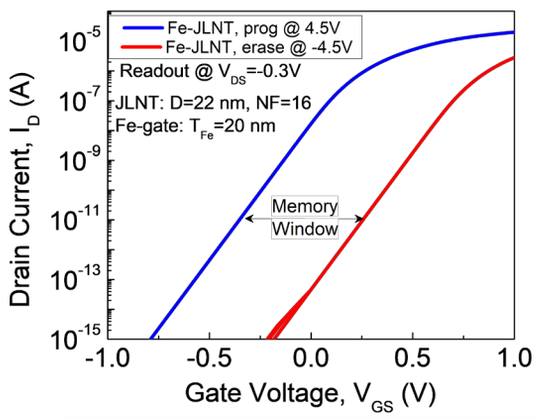


Fig. 3: Simulated predictive program and erase characteristics of a ferroelectric junctionless nanowire transistor with FE capacitor calibration data.

Back-Bias RFETs on an Industrial 22 nm FDSOI Platform

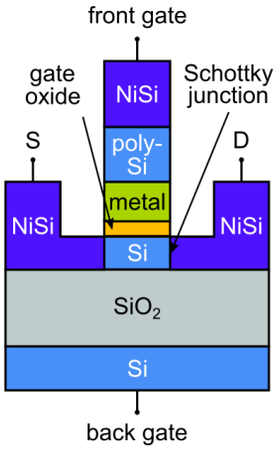


Fig. 1: Sketch of the back-biased reconfigurable transistor (BB-RFET) requiring only one front gate and utilizing the back gate bias (BB) for mode selection. NiSi contacts are driven inside the channel.

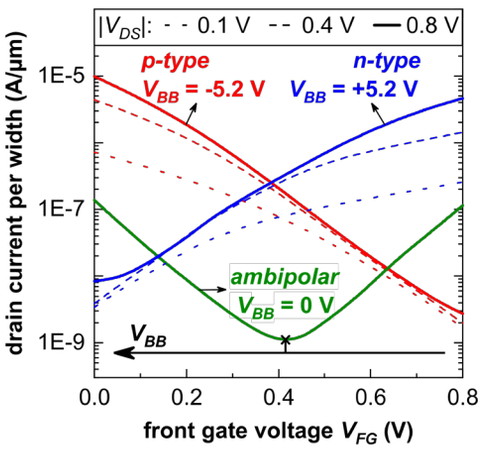


Fig. 2: Measured transfer characteristics of a BB-RFET with patterned width of 80 nm and 20 nm. P-type, n-type and ambipolar modes are selected by the applied back bias.

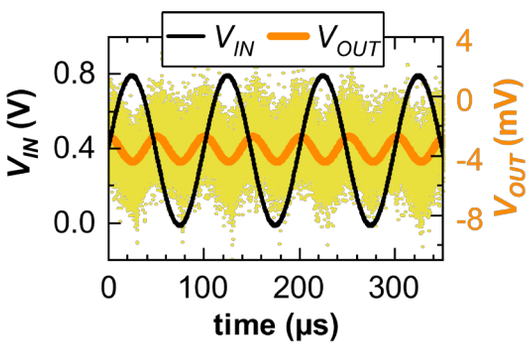


Fig. 3: Frequency doubling based on a BB-RFET. For an input frequency of 10 kHz the output signal oscillates with 20 kHz. Setup noise is indicated in yellow.

One focus of NaMLab's research is the transfer of promising research results into real world applications. NaMLab is currently working together with it's industrial partner GlobalFoundries towards the integration of the RFET concept into 22 nm fully-depleted-silicon-on-insulator (FDSOI) as potential add-on technology. Here, the structural similarities of RFETs with FDSOI transistors are beneficial for the ease of co-integration. In principle, the same materials and processes can be used and only a small number of additional uncritical lithography masks are needed.

In this framework a new back-bias (BB)-RFET device concept was proposed. Instead of multiple independent front-gates, the inherently present back-gate is used for programming between n-type and p-type characteristic, thus making the device fully compatible with the 22nm CMOS technology platform. Most process integration modules are shared with the n-FETs, such as STI, hybrid etch, gate-first high-k metal gate (HKMG) front gate integration, and the complete BEOL. Modified S/D terminals are used to create silicide-to-semiconductor junctions in close proximity to the doping-free channel region (Fig.1).

In the BB-RFET concept, we exploit the body-bias effect in FDSOI to adjust the carrier transport controlled by the front gate (FG) electrode. Different to other concepts both front and back gate couple capacitively to the whole channel region. The applied V_{BB} defines which charge carriers are injected into the active region for a given bias point of the front gate. This way, the whole transfer characteristics are shifted reversibly between the three different operation modes: p-type, ambipolar, and n-type, as shown in Fig. 2. The dynamic programmability between p- and n-configuration enables to map the device functionality after fabrication. Complementary inverter behavior has been demonstrated experimentally.

The new device concept is also interesting for analog signal processing in wireless communication or integrated sensing systems. A single transistor can be used for frequency doubling by exploiting the symmetric parabolic shape of the ambipolar mode, as illustrated in Fig. 3. First, the front gate is DC-biased at the minimum conduction point V_{MIN}. Then, a sinusoidal signal with a frequency of 10 kHz is superimposed at the gate, resulting in a doubled frequency of the output signal (20 kHz) compared to the input signal. The exact V_{MIN} can be tailored by the applied back-bias. In addition, a digital modulation of the back-bias allows to select either multiplication or transmission of the input frequency. Currently, the concept is further developed in order to yield higher functionality.

Cooperation: Globalfoundries Fab 1 Dresden

Publications: C35, I11

Contact: Dr. Jens Trommer

Resistive Switching Devices

The central aim of the research on Resistive Switching Devices is the development of materials and device structures, capable of changing their electrical resistance or capacitance by applying external voltages. The resistive memory device – the so called ReRAM – is one of the po-tential candidates for the realization of novel memories or storage class memory, since it is characterized by very fast access times, non-volatility, and low power consumption. A further interest for the adoption of these devices - which in the context of electronic circuit theory are also referred to as memristors - is the application of such reconfigurable devices in neuromorphic nano-circuits, exhibiting the unified functionali-ty of logic and memory in one device. NaMLab's activities cover the dep-osition and modification of dielectric thin films and electrode layers, the physical and electrical characterization as well as the modeling of the switching properties.

NaMLab's research focuses on niobium oxide (NbOx)-based resistive switching devices. By variation of the fabrication process, electrode ma-terials and thin film composition a large variety of different switching characteristics could be obtained. Fig. 1 depicts the measured I(V)-characteristics of a niobium oxide / aluminum oxide-based bi-layer de-vice. The analogue resistive switching behavior results in a smooth hys-teresis curve that allows storage of multiple resistance states. The re-sults of the temperature-dependent measurements are used to study the electrical conduction mechanisms. A comprehensive understanding of the underlying physical mechanisms is an important prerequisite for further device optimization targeting a large Ion/Ioff ratio. The electrical switching kinetics are characterized by pulsed and transient characteri-zation methods. Fig. 2 depicts the measured on-current after application of set-voltage pulses with increasing pulse width at an amplitude of -3V. From such measurement series we deduce the time constants that allow the differentiation between different charge-trapping- or ion-movement-based switching mechanisms. The relatively long time-constants are interesting for the application of these devices in neuro-morphic circuits that operate at biological time constants in the ms-range.

A joint technology and design co-development is of utmost importance for advancing the technology readiness level of a novel device from the proof-of-concept (TRL 3) via demonstration of the principle towards the component validation in a laboratory or even industry relevant envi-ronment (TRL4-5). In order to bridge the gap between the laboratory research and first industrial tests, NaMLab develops hybrid integration concepts where the novel devices are integrated into the back-end-of-line (BEOL) of standard CMOS chips (Fig. 3).

Cooperation: TUD, GLOBALFOUNDRIES, IPMS, IHP

Publications: J42, J85, C18, C26, M3

Contact: Dr. Stefan Slesazeck

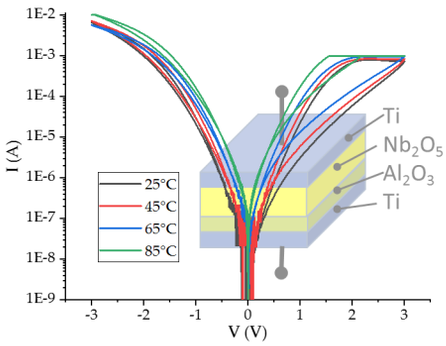


Fig. 1: I(V) characteristics at various temperatures of an analogue resistive switching device based on a niobium oxide / aluminum oxide bi-layer stack.

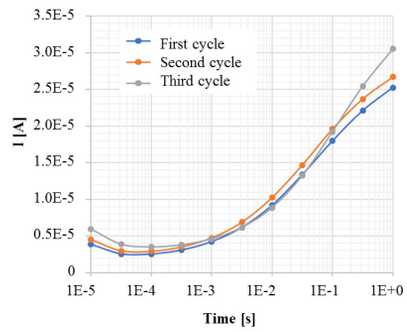


Fig. 2: Switching kinetics of the analogue resistive switching device. Voltage pulses of -3V amplitude with increasing width are applied and the on-current is monitored.

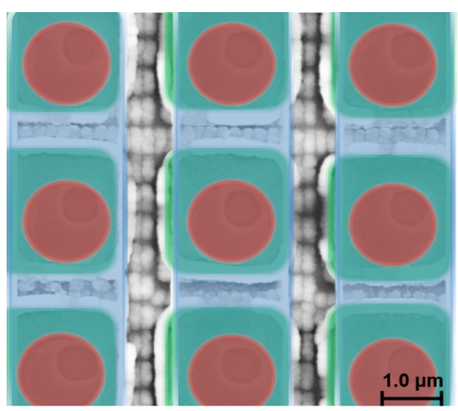
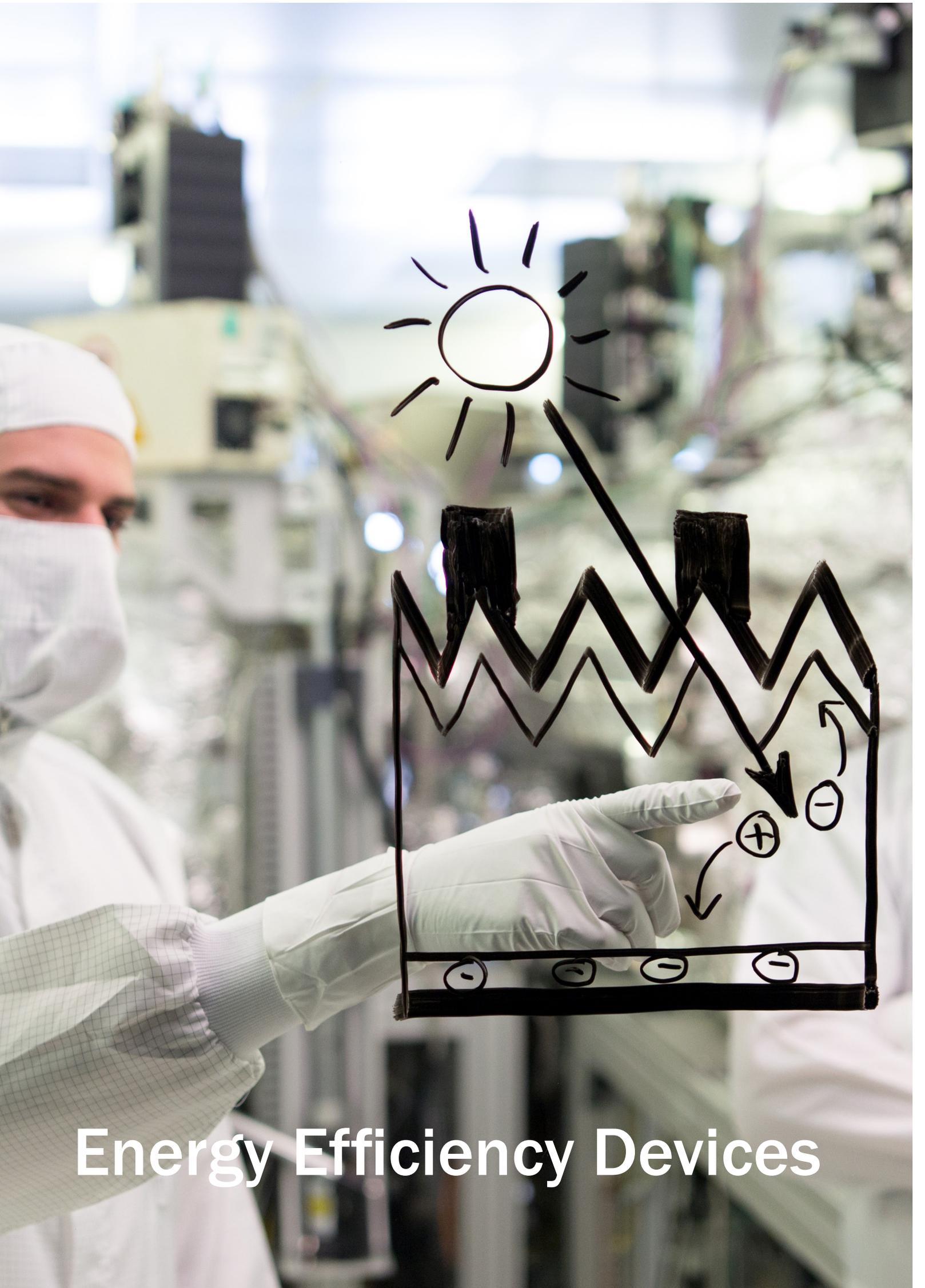


Fig. 3: Top-down SEM image of a 64kbit ReRAM test chip. In green, red and blue the bottom elecwwtrode and the top electrode manufactured at NaMLab as well as the connection of the top electrode to the source line of the underlying 28nm CMOS chip via an insulation layer are highlighted, respectively.



Energy Efficiency Devices

Si-Nanowire Electrodes For Enhanced Li Based Batteries

Lithium Ion Batteries (LIBs) have been a subject of an intense research since their first commercialization more than 25 years ago. The development of high capacity electrode materials is the most critical limiting factor to progress to next generation batteries for electric vehicles. As an anode material, silicon exhibits an unmet high theoretical capacity (3579 mAh/g), which is ten times larger than the capacity of the state-of-the-art material graphite (370 mAh/g). However, silicon anodes experience dramatic volume change during lithiation and delithiation of more than 300%, which leads to pulverization of anode material, unstable solid electrolyte interface formation and subsequent battery failure.

At NaMLab gGmbH we are tackling these challenges by pursuing two strategic tracks. The first track is focused at the establishment of an in-situ Characterization of the solid electrolyte interface at the Si anode by employing Raman-Spectroscopy. This is a non-destructive way to determine the components of the anode, the electrolyte and their interface. It allows the monitoring of compositional and structural changes during the charging and discharging processes. Thus, the mechanisms of degradation can be investigated in real-time (c.f. Fig. 1 and Fig. 2). The second track is the development of innovative high capacity anode structures using Si nanowires and integrating them with the help of strong partners of the “Excellent Battery Center Dresden”. A stable operation of carbon coated Si nanowires (cf. Fig. 3) in a LIB with a high capacity of 4mAh/cm2 at high charge/discharge rates for more than 600 cycles has been demonstrated. As the capacity per weight is the most important criteria for batteries targeting automotive applications, the binder-free high capacity Si nanowire anodes directly grown on a light-weight carbon based current collector give a unique opportunity for ongoing studies related to the integration in cell designs for batteries.

The strong collaboration with our partners Fraunhofer IWS, IKTS, the Leibniz institute IFW and the TU Dresden within the framework of the project “KaSiLi” yielded full cells up to the pouch cell level using Si anodes involving Li-Ion and Li-sulfur chemistry and the establishment of in-situ Characterization based on Raman spectroscopy.

Cooperation: FhG IWS, IKTS, IFAM; Leibniz IFW; TU Dresden (IAC, IfWW, IOF)

Publications: J2, J12, J14

Contact: Dr. Matthias Grube

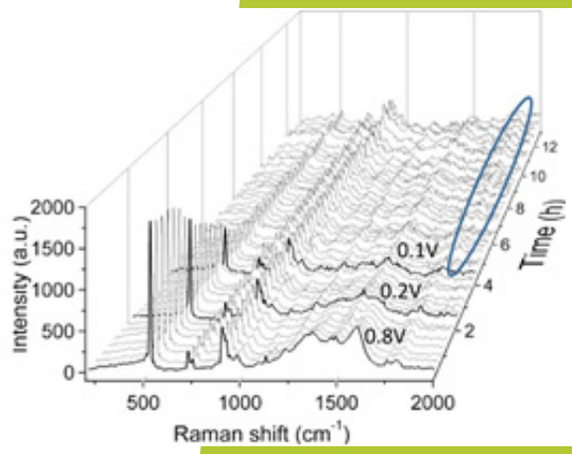


Fig. 1: In situ Raman-Analysis of a Si nanowire anode coated with pyrolytic carbon during cycling.

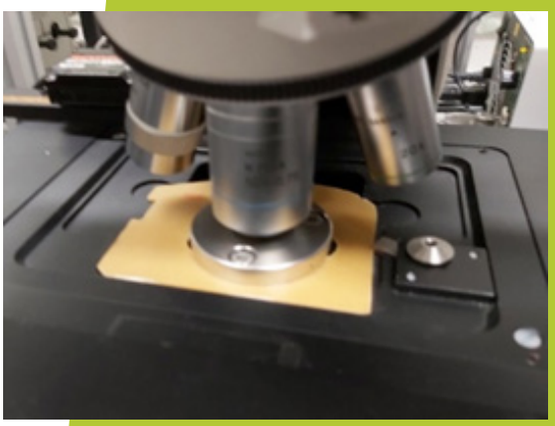


Fig. 2: Measuring cell for Raman investigations on anodes for Li-ion batteries.

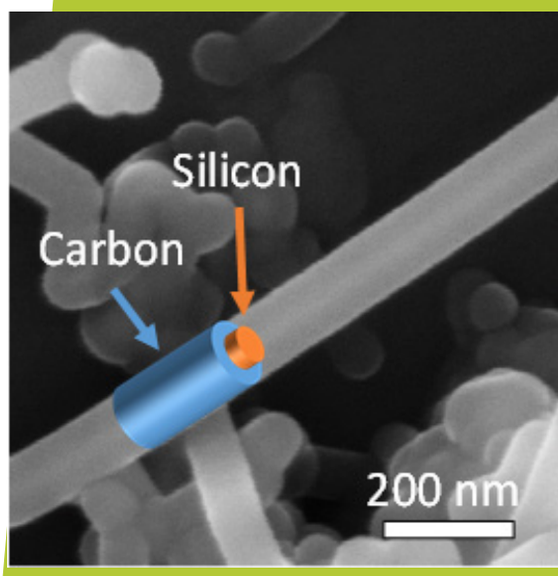


Fig. 3: SEM image of a single Si nanowire coated with an extremely uniform pyrolytic carbon layer.

Gallium Nitride Hydride Vapor Phase Epitaxy

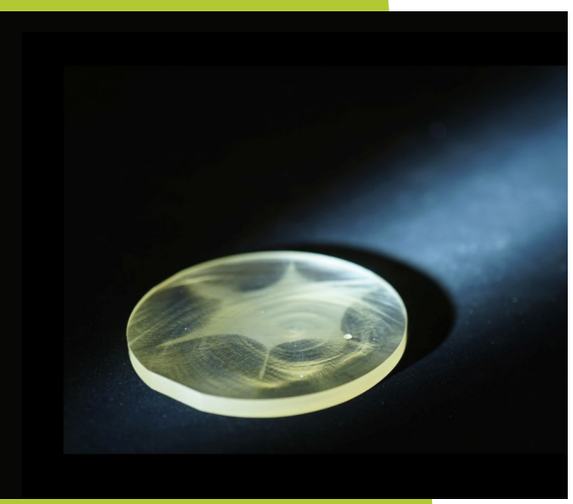


Fig. 1: Unintentionally doped (UID) 2“ round-ground GaN crystal grown on a template optimized for self-separation. It is about 5 mm thick with a smooth and specular surface.

Fig. 2: Ge-doped 2“ GaN wafer cut from a self-separated, 5 mm thick boule.

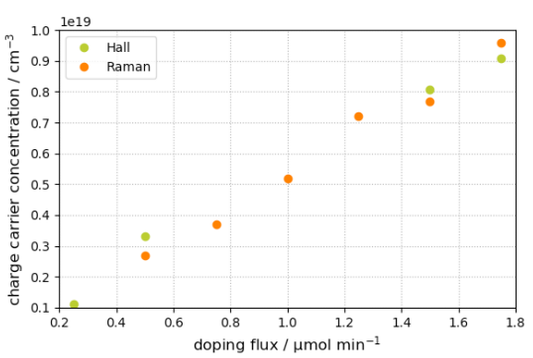


Fig. 3: Increase of free charge carrier concentration with increasing amount of supplied dopants.

Since 2011, NaMLab is belonging to a small but elite group of bulk-GaN growers. It cooperats onsite with Freiberger Compound Materials (FCM) in Freiberg and owns a modified and optimized state-of-the-art vertical HVPE reactor. The focus of the research and development is on the growth of several millimeters thick GaN-crystals (Fig. 1). So far, crack-free 2” crystals can be grown reliably and cut into distinct wafers (Fig. 2). Besides upscaling to higher diameters, the optimization of the lattice properties, e.g. the lattice bow, and the electrical properties, which range between n-type and semi-insulating, is of major scientific interest.

Due to the hetero-epitaxial approach of the HVPE process, bowing of the crystallographic lattice planes towards the crystal edge can not be avoided in principle. While the reported value for the radius of curvature typically is in the range of single meters, recent developments and tool reliability improvements promise a tremendous increase and, thus, superior lattice properties.

Mainly Silicon (Si) and Germanium (Ge) were used as dopants to achieve a distinct n-type conduction above the unintentional doping level with charge carrier concentrations not larger than 5 x 10^{16} cm^{-3}. A gaseous dopant chemistry is utilized for Si, while a solid-state meth-od can also be applied for Ge. A more controlled intake is possible by introducing a bubbler setup using GeCl4. Here, very high charge carrier concentrations up to 1 x 10^{19} cm^{-3} are already possible (Fig. 3). The drawback, similar to Si doping, is an increased lattice bow with higher doping concentrations.

In both cases, the distribution of the charge carrier concentration perpendicular to the crystal surface is uniform. The distribution along the surface is more inhomogeneous for Ge-doped than for Si-doped GaN. In the future, the uniformity improvements for Ge doping will be of particular interest since higher free charge carrier concentrations might be achievable for this dopant.

In addition, also other doping methods like doping with metal-organic precursors or soluble solids in a liquid gallium source to achieve semi-insulating like GaN:Fe via Cp_2Fe (ferrocene) or GaN:Mn via solid Mn have been established and investigated.

The doped crystals and corresponding wafers are also monitored with respect to their lattice and mechanical properties in order to investigate the influence of the dopants. Future investigations will concentrate on improving crystal lattice bow, dopants incorporation, and crystal diameter further.

Cooperation: Freiberger Compound Materials GmbH

Publications: C15

Contact: Dr. Sven Jachalke

Gallium Nitride MBE & Fundamentals

During the past years the growth of ultra-pure GaN/AlGaN heterostructures with atomically-smooth interfaces and surfaces on bulk GaN by molecular beam epitaxy (MBE) was established. The resulting layer stacks are a perfect reference system for fundamental material investigations as well as a test ground for novel electrical and optical device concepts. In particular, after lowering the unintentional oxygen background in the grown layer stacks to the irreducible level of 2e16 cm^{-3} it was observed, that a 2-dimensional electron gas (2DEG) is not present in the dark and at room temperature. However, such a 2DEG can be generated by illumination with ultra-violet light (Fig. 1) and electrostatically. The latter immediately results in normally-off operation of lateral field-effect transistors (FETs) in the dark (Fig. 2). For lateral FET operation the overlap of the gate metal and the source and drain contacts is vital to electrostatically address the vicinity of these contacts. Under UV-illumination on the other side, these devices operate normally-on. Microscopically the absence of a 2DEG is attributed to Fermi level pinning at an unknown deep acceptor. After blanking the UV light the 2DEG vanishes again. This effect represents a route towards novel GaN-based normally-off and UV-sensitive device schemes.

The situation changes at low temperatures. Here the 2DEG persists after blanking the UV light, which allows for investigating quantum transport phenomena in this steady state. Quantum transport is fully developed at 2 K, which is manifested by the onset of Shubnikov-de Haas oscillations in the longitudinal magneto-resistance below 2 T, the observation of odd Landau level filling factors at 6 T and the quantization of the Hall voltage (quantum Hall effect) at small even filling factors (Fig. 3). Originally the growth on bulk GaN with a low threading dislocation density (TDD) < 10^7 cm^{-2} was predicted to boost the low temperature 2DEG mobility due to the reduction of Coulomb scattering originating from charged dislocations. Our data prove that this is not the case and the mobility only amounts to ~ 20.000 cm^2/Vs, despite the pronounced quantum transport features. The analysis of the quantum and transport lifetimes (τ_q and τ_t) rather points at a different origin for scattering than the charged dislocations. A small ratio τ_t/τ_q < 10 implies efficient large angle scattering, caused e.g. by a charged point defect inside the grown GaN material. A good candidate for such a charged point defect could be the above mentioned deep acceptor at an energetic position of ~ 0.8 eV above the valence band maximum.

Cooperation: MPI CPfS, Russian Academy of Sciences, Technische Universität Dresden (IHM), Czech Academy of Sciences

Publications: J13, J34, J81

Contact: Dr. Stefan Schmult

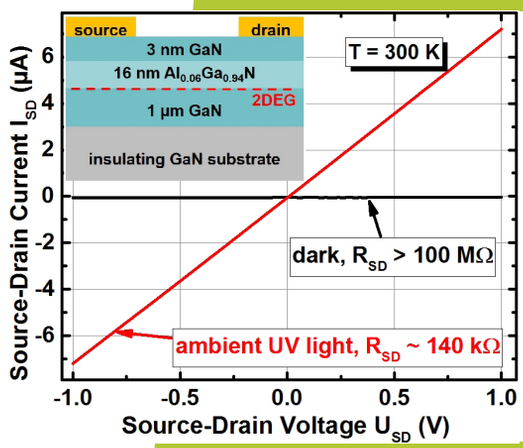


Fig. 1: Lateral conductivity of an ultra-pure GaN/AlGaN layer stack at room temperature in the dark and under UV-illumination. The low conductivity in the dark implies, that a 2DEG is not present here, while under illumination with UV light a conductive channel is generated.

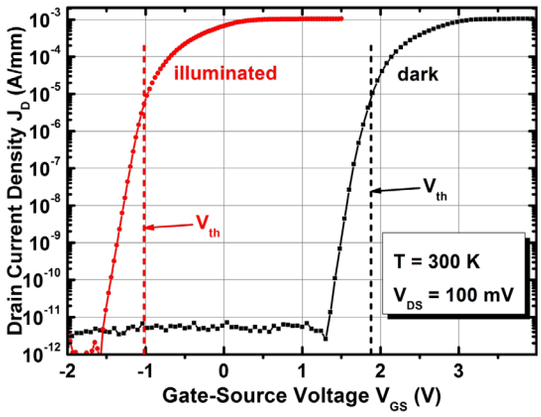


Fig. 2: Normally-off and normally-on operation at room temperature in the dark and under UV-illumination, respectively, of a lateral FET fabricated from the ultra-pure GaN/AlGaN heterostructure presented in Fig. 1. The I_{on}/I_{off} ratio is larger than 10^8 in both cases.

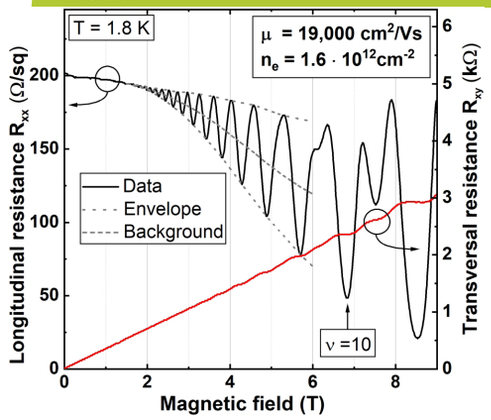
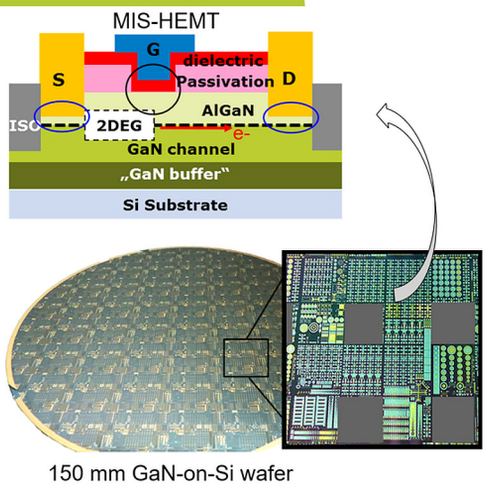


Fig. 3: Longitudinal and transversal magneto-resistances at low temperature of the GaN/AlGaN heterostructure in Fig. 1. Pronounced quantum transport is reflected by Shubnikov-de Haas oscillations commencing below 2 T, the observation of odd Landau filling factors at 6 T and the quantization of the Hall voltage (quantum Hall effect) at 7 T.

Gallium Nitride Based Device Technology



150 mm GaN-on-Si wafer

Fig. 1: Cross section MIS-HEMT device, process modules under investigation marked with circles. Below: image of processed 150 mm GaN-on-Si HEMT wafer with zoom in test chip die.

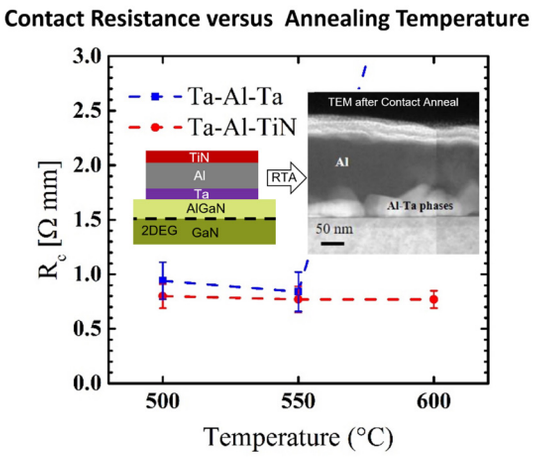


Fig. 2: Contact resistance of Ta/Al-based ohmic con-tact to AlGaN/GaN 2DEG versus annealing temperature applied for contact formation. Inset shows TEM image of contact region.

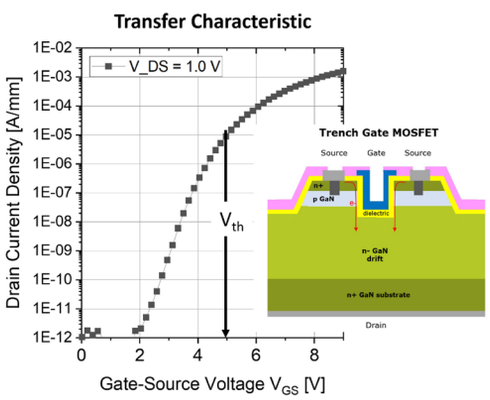


Fig. 3: Cross sectional schematic of vertical MOSFET with trench gate configuration. Transfer char-acteristic of vertical MOSFET at VDS=1.0V. Drain current scaled on channel width in trench gate. True normally-off device operation with threshold voltage ~5V is demonstrat-ed.

The III-V compound semiconductor Galliumnitrid (GaN) has outstanding intrinsic material properties for power device applications. NaMLab's GaN device development is focused on electronic power devices with high voltage operation. The High-Electron-Mobility-Transistor (HEMT) concept features a 2 dimensional electron gas (2DEG) at the Al_xGa_yN/GaN heterojunction interface. It represents the backbone of GaN power transistors with planar or lateral current conduction close to the wafer surface. The material for industrial fabrication consists primarily of MOCVD grown GaN on Si(111) substrates with diameter of 150 mm or 200 mm.

A HEMT technology based on contact lithography for 150 mm wafers is utilized for material characterization and device development in co-operation with external partners (Fig.1). NaMLab is working on process modules for improving overall device performance, stability and reliability. We investigate the integration of a high-k dielectric material underneath the gate electrode to fabricate a Metal-Insulator-Semiconductor (MIS)-HEMT. Process engineering on the (Al)GaN surface prior to the deposition of the dielectric as well as post-annealing of the gate structures improves importantly the threshold voltage stability by reduction of charge trapping effects at the dielectric/GaN interface. The second development is related to an alternative ohmic contact module based on Ta/Al metal bilayers compared to the mainstream Ti/Al contacts. Material engineering resulted in low-resistance Ta/Al/TiN-ohmic contacts (Rc < 1 Ω.mm) at much lower annealing temperatures (≤ 600 °C), which are gold-free and enable a higher integration flexibility (Fig.2).

Another development path is related to vertical GaN power devices, having the advantage of an almost area-independent scaling of the breakdown voltage. NaMLab is developing vertical GaN MOSFET devices with trench gate configuration and device channel along the vertical sidewall of the trench (Fig 2.). After first implementation of the process technology on semi-vertical devices due to better material availability, the process integration has been adapted to full vertical devices with backside contact on 2-inch free-standing GaN substrates. Device functionality with threshold voltages in an appropriate range (V_{TH} > 3V) was demonstrated (Fig.3). Utilizing a drift layer with a thickness of 10 µm and optimizing the lateral termination structure pushed the breakdown voltage beyond 800 V. Current work addresses the trench gate module to increase the current drive and reduce the on-state resistance of the MOSFET as well as increasing the breakdown behavior. Besides, the focus on device level shifts from single trench cell test devices to power demo-devices with multiple gate trenches connected in parallel.

Cooperation: Freiberger Compound Materials, X-FAB, TU Dresden IHM, TU-BA Freiberg, RWTH Aachen.

Publications: J5, J47, C15, C19, P6

Contact: Dr. Andre Wachowiak

Versatile Passivation Layers For Silicon Solar Cells

State-of-the-art silicon solar cells require excellent surface passivation. Al_2O_3 and Si_3N_4 are the standard materials for silicon as high-quality passivation. At NaMLab, those materials were further developed to multi-oxide nanolaminates with tailored material properties. These layers enhance the classical surface passivation and open the field of conductive passivation for next generation PERC (Passivated Emitter and Rear Contact) cells.

There are two major advantages related to passivating contacts. On the one hand, opening the classical passivation layer in order to contact the cell itself involves process steps, which consume high amounts of energy. These process steps would be obsolete. On the other hand, losses attributed to the lateral diffusion of charge carriers towards the local contact openings and recombination of charge carriers at the openings itself will be reduced (c.f. Fig. 1). Therefore, the efficiency of the cell will be increased. Four major criteria have to be fulfilled: The contacts have to exhibit a very high transparency for visible light, a good passivation behavior, a good conductivity and have to be compatible to the existing PERC process flow. Since 2016 NaMLab is investigating oxide layer stacks as potential candidates for this purpose. The main concept consists of a passivating tunnel oxide (Al_2O_3 or $H:Si_xN_y$) and a transparent conducting oxide (doped TiO_x). After performing an enhanced engineering of the nanolaminates (c.f. Fig. 2), it was possible to realize layer stacks, which fulfil the afore-mentioned criteria for the p-contact as well as the n-contact. There-fore, a solar cell as sketched in Fig. 1 can be manufactured. Currently, NaMLab is integrating those contact stacks in Si solar cells as shown in Fig. 3 to verify their potential for a commercial application.

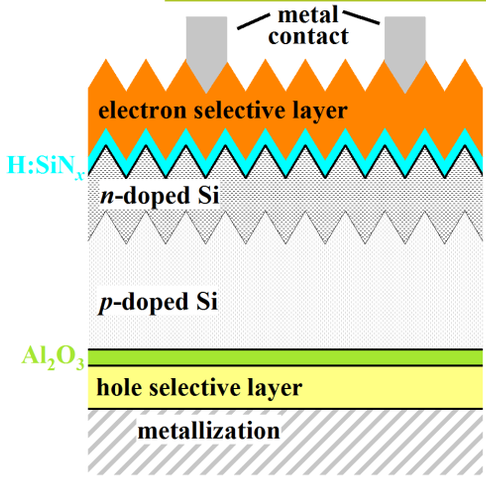


Fig. 1: Sketch of a next generation PERC cell with full-area passivating contacts.

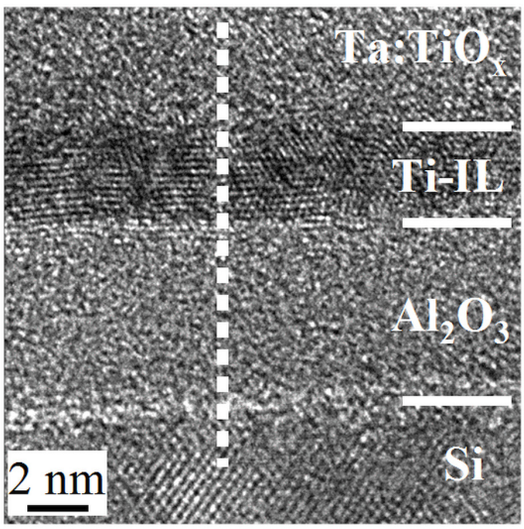


Fig. 2: TEM image of a nanolaminate made of Al_2O_3 and Ta doped TiO_x.

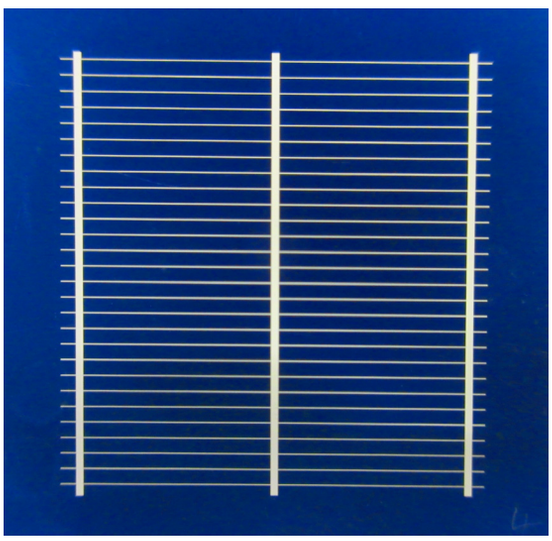


Fig. 3: Photograph of a solar cell with a passivating contact at the front side. The small silver lines are bus bars for extraction of the gen-erated current. The metal grid covers an area of 2 cm².

Cooperation: Technische Universität Dresden (IHM), FAP GmbH, Meyer Burger AG, Solayer GmbH

Publications: J39, J50, J84

Contact: Dr. Matthias Grube

Competences

Electrical Characterization

Electrical measurements are essential for the characterization of the materials that are used to create electronic devices and circuits. NaMLab adopts a broad spectrum of electrical measurement techniques and analysis methods for device characterization. This includes capacitance measurements, such as C(V), C(T) and C(f), current measurements with down to femto-ampere resolution at temperatures between 5 K and 450 K and voltages up to 3000 V. Samples can be analyzed by direct probing on wafer level using single probes, probe cards or special RF-probes. Package level testing can be performed for long-term reliability characterization or for the adoption of our devices in test-circuits. In addition, carrier lifetime measurements are available on substrates with Microwave Detected Photoconductivity.

The established methods at NaMLab include:

- Analysis of single memory cells (memory window, retention, endurance,...) by static and pulsed measurements
- Determination of transistor and capacitor characteristic curves by C-V and I-V measurements
- Determination of sheet resistance for thin layers.
- Determination of doping profiles by scanning spreading resistance Microscopy (SSRM)
- Reliability characterization of dielectric and transistors
- Defect characterization by charge pumping and charge trapping analysis and defect spectroscopy
- Measurement of charge carrier mobility with Hall and split-C(V)
- Pulsed and high frequency measurements
- Power device characterization

Electrical material characterization is regularly used to attain fast feedback loops, thus supporting the material development. Fig. 1 shows a sample containing memristor devices that were manufactured at NaMLab. The memristors are connected via needles. The sample is placed on an isolating chuck for low-noise measurements.

Besides the utilization of standard single device measurements, custom-ized characterization setups are created at NaMLab. This work includes the development of special circuits and non-standard test environments.

Fig. 2 shows the test setup for FeFET-based compute-in-memory test structures using an FPGA board. The FPGA controls the digital interface to an image-filter accelerator to be operated in real-time video-applications.

Fig. 3 depicts the measured bit-map of a 16kBit 2T1C FRAM array. The ferroelectric capacitors were processed at NaMLab on top of a 28nm CMOS chip that was manufactured by GF. Brighter color indicates a larger leakage current in the ferroelectric capacitors. The characterization of array-test structures allows statistical reliability investigations and the observation of effects that are barely accessible in single device struc-tures.

Contact: Dr. Stefan Slesazeck

Fig. 1: Low-noise measurements on an isolating chuck .

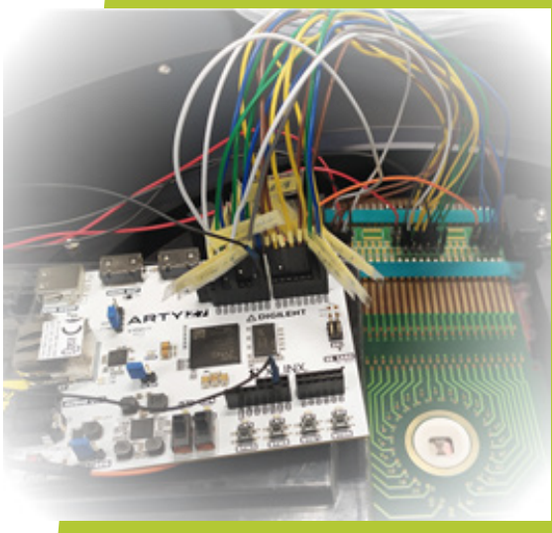


Fig. 2: FeFET-based compute-in-memory circuits that were manufactured on a 300mm wafer are probed using a needle card and are connected to an FPGA development board for digital control.

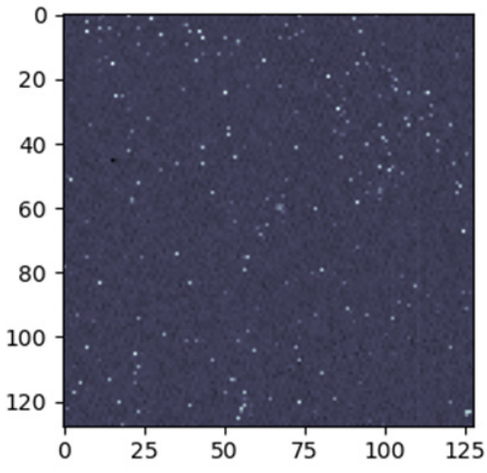


Fig. 3: Measured leakage current map of ferroelectric capacitors in a 16kBit sub-array out of a 64kBit 2T1C FeRAM test chip manufactured at NaMLab.

Physical Characterization

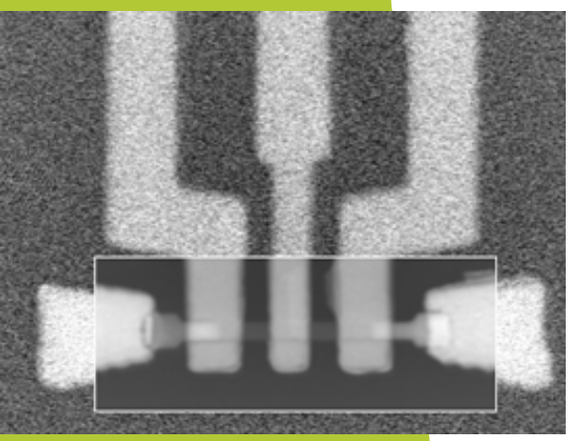


Fig. 1: SEM image of $NiSi_x$ contacts below metal gates imaged with an AsB detector.

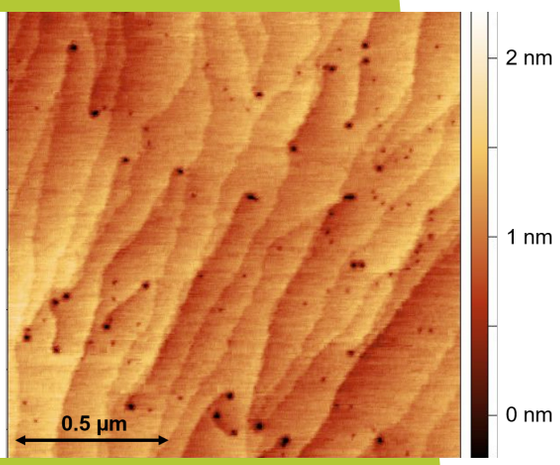


Fig. 2: Surface topography of MOCVD GaN with monolayer stepped terrace structure. Pits of shallow (deeper) depth indicate end points of threading edge (screw + mixed) dislocations.

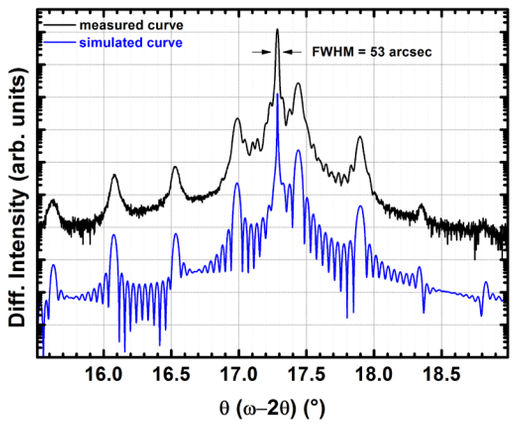


Fig. 3: Measured and simulated high resolution X-ray diffraction pattern of AlGaN/GaN superlattices grown by molecular beam epitaxy at NaMLab.

NaMLab hosts a dedicated physical characterization toolpark to supplement its core expertise in state-of-the-art material development and electrical characterization. One focus of the physical characterization at NaMLab aims to provide fast-feedback to the technology development in the cleamroom and at research partners.

Two high-resolution scanning electron microscopes (HR-SEM) are capable of providing high magnification images down to 10 nm resolution. Our new angle-selective-backscattered electrons detector (AsB) allows to obtain superior material contrast with respect to conventional imaging. Moreover, high channelling contrast can also be achieved, yielding more detailed crystallographic information. A possible application is the localization of nickel silicide junctions placed below metal gates shown in Fig. 1. The high material contrast delivered by the detector allows to precisely image the sharp junctions without saturation of the signal by the electron contribution coming from the overlying metal gates. Furthermore, one SEM is equipped with an energy-dispersive x-ray (EDX) detector to reveal chemical composition of the samples covering almost the entire periodic table. The EDX system is coupled with a newly-aquired Electron Back-Scatter-Diffraction (EBSD) detector, to also yield localized information about crystal structure, phases and textures of nanoscale materials.

The atomic force microscope (AFM) is routinely used for mapping the surface topography by using contact or tapping mode. Resolution in the order of 2 nm in the scanning direction (X/Y) and below 0.1 nm perpen-dicular to the scanning direction (Z) can be realized, shown at an exam-ple of an epitaxial grown GaN surface in Fig. 2. At NamLab a big variety of special measurement technique is used with a great expertise such as scanning Spreading Resistance Microscopy (SSRM) to map the spatial dopant distribution, conductive AFM (C-AFM) for measuring local leak-age current density, piezo fowrce microscopy (PFM) for analyses of piezo-electric materials by measuring the vertical displacement of the AFM tip in response to an electrical excitation of the sample.

A multifunctional X-ray diffractometer (XRD) is used to yield information about crystal structure. The tool has a resolution of < 40 arcsec and is used for phase analysis, measuring reciprocal space maps, determining the composition of alloys, layer thickness and stress state. A high-resolution X-ray diffraction measurement on a AlGaN/ GaN superlattice structure is shown in Fig. 3.

Contact: Dr. Jens Trommer / Dr. Andre Wachowiak

Optical Characterization

A key pillar in understanding fundamental semiconductor material properties and device performance is optical characterization. At NaMLab, various techniques such as photoluminescence (PL), Raman and Fourier transform infrared spectroscopy are applied to determine defect types and energies, phonon energies and transmission and reflection characteristics in semiconductor materials. Furthermore, photoactive electrical devices can be characterized.

One focus of NaMLab's optical activities over the past two years was on optical studies of galliumnitride (GaN) material with its large band gap of 3.4 eV employing low-temperature PL measurements. As a key component of this set-up, the old monochromator was replaced by a high-resolution HORIBA FHR1000 equipped with a CCD camera (Fig. 1). As a consequence, data acquisition time was drastically reduced. Immediately after installation an energy resolution < 100 µeV could be demonstrated.

An open question since the discovery of photoconductivity in GaN/AlGaN 2DEGs was the energy threshold of the optical response. A Hall bar fabricated from an ultra-pure GaN/AlGaN heterostructure grown by MBE was used as a photodetector and white light dispersed through the monochromator served as wavelength-specific excitation. In this experiment it was concluded, that a 2DEG is only generated at excitation energies of the GaN band gap and above (Fig. 2).

With the Raman set-up, degradation mechanism of silicon anodes integrated in lithium ion batteries were extensively investigated in situ during Si lithiation/delithiation. With these measurements, a relationship between structural and electrochemical properties over electrode cycling have been established. As a result, amorphous as well as liquid and transient species in a battery cell were observed (Fig. 3).

In summary, established optical methods at NaMLab include:

- Low-temperature photoluminescence (15 – 300 K) in the UV – visible spectral range (340 nm – 800 nm) with UV (325 nm) laser excitation
- Spectral response with and without bias illumination for photosensors and solar cells
- Micro-Raman mapping with 457 and 514 nm excitation wavelength (spatial resolution: 1 µm) for e.g. local strain analysis
- IR and VIS-NIR ellipsometry and VIS-NIR reflectometry
- Microwave detected photoconductivity for 2D mapping of minority carrier lifetimes in silicon
- Fourier Transform Infrared (FTIR) Spectroscopy (2000-20000 nm) for analyzing lattice and molecular vibrational bands

Cooperation: TU Dresden (IHM), Russian Academy of Sciences, CfaeD TU Dresden, IfWW TU Dresden, IFW Dresden

Publications: J12

Contact: Dr. Matthias Grube, Dr. Stefan Schmult

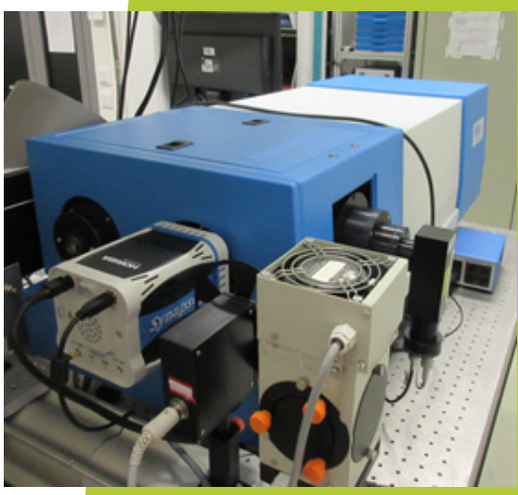


Fig. 1: A HORIBA FHR 1000 high resolution monochromator equipped with a CCD camera replaced the more than 20 years old system.

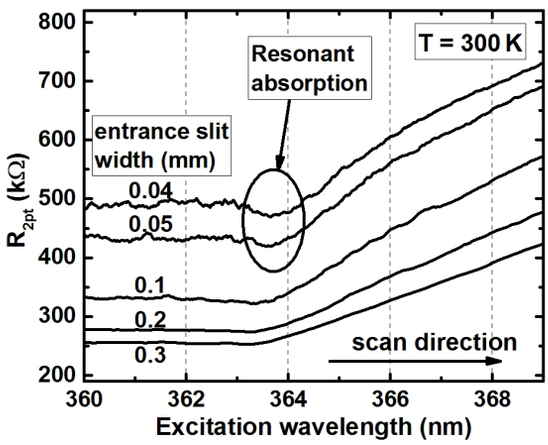


Fig. 2: Wavelength-dependent conductivity of an ultra-pure GaN/AlGaN heterostructure grown by MBE. The threshold for the generation of a 2DEG is the GaN band gap energy.

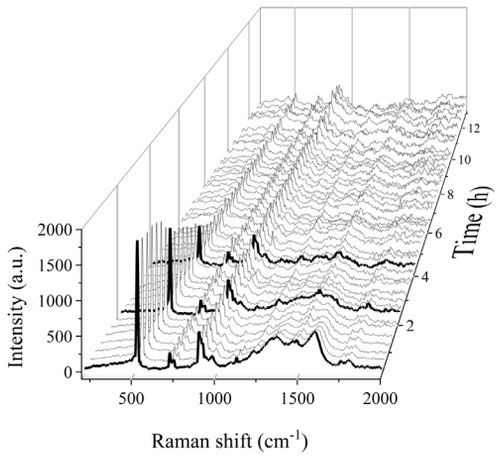


Fig. 3: Raman data obtained in NaMLab's optical lab reveal straightforward different signatures for various battery anode materials and allow to characterize in-situ degradation processes of these materials.

Device Reliability

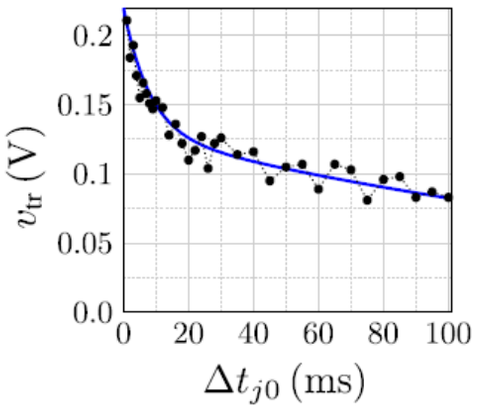


Fig. 1: Measured trap discharging process of a carbon nanotube FET obtained from pulsed measurements. Data is fitted by a compact model with two trap-related emission time constants.

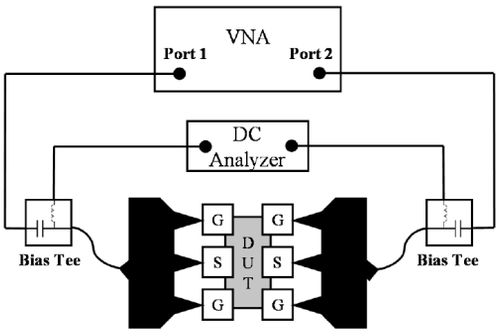


Fig. 2: Experimental setup used for S-Parameter based on-the-fly BTI characterization with externally controlled RF and DC analyzers.

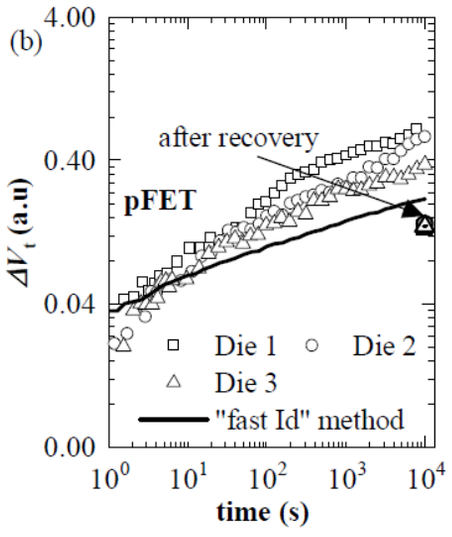


Fig. 3: Extracted threshold voltage shift measured in direct S-Parameter method as compared to 'fast ID' method. The dotted symbols depicts the shift after a few minutes of recovery.

The development of novel microelectronic devices as well as the scaling of existing devices concepts is tightly linked to the availability of mature and reliable integration of new dielectrics. On the nanometer scale those materials act as gate insulator, stress or strain layers or memory dielec-trics. NaMLab performs electrical stress measurements on a large variety of devices to assess the reliability of the used dielectric materials. More-over, simulation and modeling of the different degradation effects give deeper insight into the physical mechanisms. For an example, we have conducted a study reversible capture and emission processes of inter-face and oxide traps in a carbon nanotube (CNT) FETs by using pulsed measurement schemes. The measured data was then fitted by one of our partners using transient simulations with a CNT-FET compact model containing a trap modeling adjunct network with different time con-stants for capture and emission of processes exemplarily shown in Fig. 1.

In face of the increasing complexity of power devices or high perfor-mance logic devices any compromise in reliability is not acceptable. Es-pecially for high dielectric constant gate insulators, the fundamental understanding of bias temperature instability (BTI), hot carrier injection (HCI), stress induced leakage currents (SILC), and time dependent dielec-tric breakdown (TDDB) are of major interest. To further deepen the un-derstanding of use-case realistic stress conditions we put additional fo-cus on the assessment of circuit reliability. That is, besides the standard reliability tests on single devices that are typically performed with high statistics at our partners premises, more advanced and time consuming characterization methods are investigated at NaMLab.

The growing interest in high speed and RF technologies assert for the importance of reliability characterization beyond the conventional DC or AC methodology. Power amplifiers for example that are adopted to real-ize on-chip transmitters have to operate stable at frequencies well be-yond the GHz range. Thus, the correct understanding of degradation mechanisms that affect the RF device parameters becomes increasingly important. Often new methods have to be established to yield the de-sired information. For example, we have proposed a new S-Parameter based BTI characterization method, whose setup is shown in Fig. 2. This technique distinguishes itself from other BTI characterization methods, that it does not constitute any recovery component as the degradation is monitored without disengaging the stress condition while using a standard RF measurement setup. Exemplarily, the threshold voltage shift of a p-FET under BTI stress conditions is shown in Fig. 3. Data from S-Parameter based method is compared to the classical 'fast ID' meth-od, as well as to the data achieved after a recovery time of a few minutes.

Publications: J86, C2

Contact: Dr. Stefan Slesazeck

Sample Preparation

The research programs at NaMLab require very specific preparation of samples. The sample preparation ranges from low-complexity ap-proaches of 1D layer stack depositions up to complex BEOL-post pro-cessing of functional devices on top of CMOS substrates using up to 5 lithography steps.

This preparation can include deposition of thin films and layers, thermal treatment of samples, patterning by lithography and etching, as well as sample cutting, grinding, polishing and engravings. For this purpose, the 330 m² ISO class 6 cleanroom facility includes various types of deposition tools: physical vapor deposition (PVD), atomic layer deposition (ALD), chemical vapor deposition (CVD), and molecu-lar beam epitaxy (MBE). Post deposition anneals can be performed in various hot and cold wall ovens, which cover a temperature range for room temperature up to 1200 °C. There are fast ramping Rapid Thermal Processing machines available as well as furnaces for long-term treatment. Structures in the range of micro- and nanometers can be manufactured by employing shadow masking and lithographic methods like electron beam (Fig. 1) and laser lithography. The re-moval of the material includes wet chemical and reactive ion etching (RIE).

Additional requirements of the scientific processing is adapting wafer geometries, chip dicing and creation of process compatible gadgets e.g. for sample handling. Therefore, NaMLab provides several tools to meet these requirements. A Synova LSC 300 W Laser cutter (Fig. 2) is located in NaMLab's clean room. It offers the possibility to process wafers with diameters up to 300 mm and substrate thicknesses up to 1 mm. Via a CNC based vacuum chuck any 2-dimensional shape can be produced. This technique is used for dicing silicon wafers or cutting out small pieces without destroying processed and reusable wafers.

For cleaning and wet chemical treatment of samples, NaMLab owns four wet benches equipped with overflow basins (Fig. 3). They are located in an ISO class 5 cleanroom. Ultrasonic and megasonic tools for mechanical supported surface cleaning in deionized water are in operation. Also cleaning steps like RCA clean and selective material etching can be performed.

Contact: Dr. Matthias Grube

Fig. 1: Raith eLINE Plus e-beam lithography system.

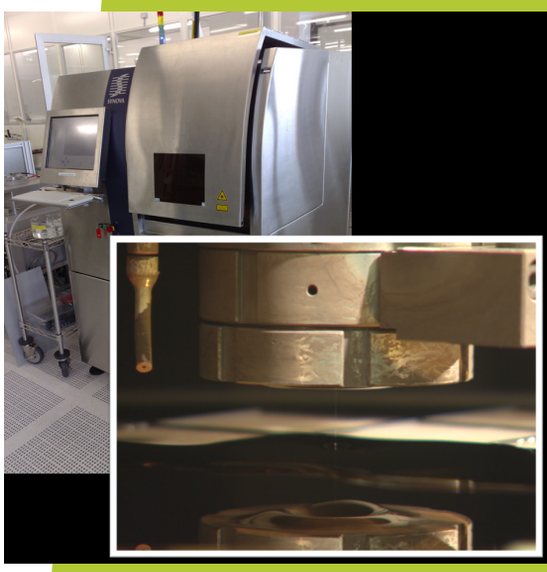


Fig. 2: Laser cutter tool for wafer cutting and engraving: Synova LSC 300W.

Fig. 3: Various possibilities to perform controlled wet chemical and reactive ion etching.

Facts & Figures

NaMLab main building.

NaMLab In Numbers

Annual Budget

The annual budget over the past six years reflects that NaMLab gGmbH has been established as an institute at full operation capacity. Any further growth of the research institute is limited by the available office space. The turnover has slightly increased in the last two years and is overall stable at about 3.9 Mio. Euros. The sum of the budget of the publicly funded projects and of contract research has been stable over the last two years. Funding by government sources has reached a baseline level and increased slightly starting in 2017. The governmental financial support accounted to about 15% to 20% of the overall revenue.

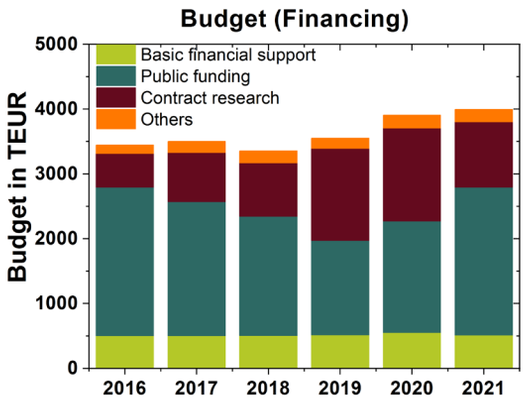


Fig. 1: Annual budget. The numbers of 2021 are preliminary. The turnover is stable and limited by the available office space.

Investment Budget

The cleanroom facility at NaMLab is conform to the highest standards of microelectronics. 250 m² of class 6 and 50 m² of class 5 clean room (EN ISO 14644) are available for experimental work. With its core competence in materials development, NaMLab runs several deposition techniques such as evaporation, molecular beam epitaxy, sputtering, chemical vapor deposition and atomic layer deposition. In total fifteen processing tools are used for research work. A wet chemistry area is equipped with cleaning, etching and spin coating processes. Two state-of-the-art electrical characterization labs for material and device characterization are equipped with 200 and 300 mm probe stations. Additional labs for optical and physical characterization are available. Additionally NaMLab chartered a lab located in Freiberg, a city close to Dresden, hosting a Hydride Vapour Phase Deposition tool and, currently in process start-up, a Metalorganic Vapour-Phase Epitaxy GaN deposition tool dedicated to research on GaN crystal growth and in the future on GaN device development.

The main investment in the last two years has been an infrastructure project financed by the EFRD fund of the European Commission and by the Free State of Saxony out of the budget approved by the Saxon State Parliament. Out of this project an E-Beam lithography writer for processing of small samples, an atomic force microscope for different type of surface investigations, a vacuum rapid thermal processing furnace and a fully automated probe-station combined with high frequency measurement capability have been installed and are already functional. Additionally a high temperature Chemical Vapour Deposition furnace and a Metalorganic Vapour-Phase Epitaxy GaN deposition tool are in process start-up. An atomic layer deposition tool for metal layers will be installed in 2022. Beside this in the last two years NaMLab invested in smaller up-grades for deposition tools and IT hard- and software financed by the basic funding of the Free State of Saxony out of the budget approved by the Saxon State Parliament.

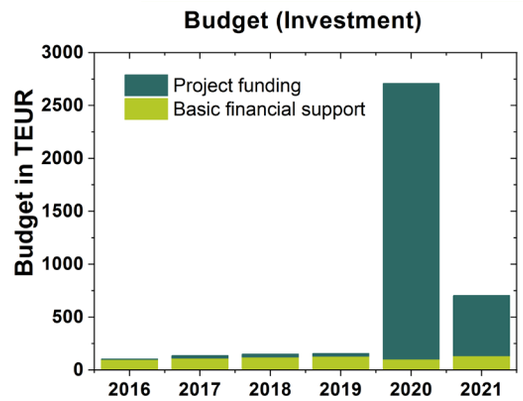


Fig. 2: Investment budget. The significant investments in the last two years have been realized by an infrastructure project financed by the EFRD fund of the European Commission and by the Free State of Saxony out of the budget approved by the Saxon State Parliament. The numbers for 2021 are preliminary.

Employment Numbers

End of 2021 the total staff counted 43 members. This includes 4 employees for administration and 3 employees for technical support and 4 senior scientists. Technicians and senior scientist guarantee an excellent and stable scientific and technical know-how basis on semiconductor devices, technology and materials for running and future projects. Currently, 15 scientists are planning to submit a PhD thesis.

Contact: Dr. Alexander Ruf

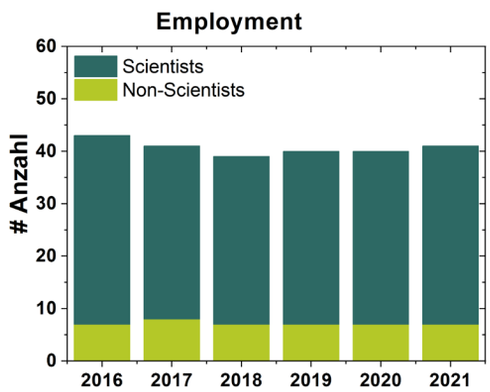


Fig. 3: Employee number development. In 2020/2021, the number of employees has been stable. Additionally, the number of master theses, project and semester works is stable at a high level (not shown).

Projects

3eFERRO (708302)

Energy Efficient Embedded Non-volatile Memory Logic based on Ferroelectric Hf(Zr)O2

BeFerroSynaptic (871737)

BEOL technology platform based on ferroelectric synaptic devices for advanced neuromorphic processors

FvIIMonti (101016776)

Ferroelectric Vertical Low energy Low latency low volume Modules for Neutral network transformers in 3D

Enkrist (03ET1398B)

Energy saving by the availability of better and cost-efficient carbide and nitride semiconductor crystals

Falcon (ZF4737101AG9)

Flash lamp based activation of passivating contacts for highly efficient solar cells

GaNESIS (16ES1090)

AlN/GaN epitaxy on silicon using reactive plus magnetron sputtering

KaSiLi (03XP0254C)

In-situ Raman investigations on anodic protective layers of silicon- and lithium-based anode materials

KI-IoT (16ME0093)

Holistic open-source platform for embedded system-on-chip

CirroStrato (16ME0210K)

Novel reconfigurable transistors for know-how protection of electronic components

Ecsel UltimateGaN (826392/16ESE0422S)

Research for GaN technologies, devices and applications to address the challenges of the future GaN roadmap

Projects

LAMP (MI 1247/12-1/2)

Locally Active Memristive Data Processing

HiMGaN (MI 1247/15-1)

Exploration of novel electrical and electro-optical device concepts and fundamental physical effects in high-quality wide band-gap semiconductor hetero structures

Homer (MI 1247/16-1)

Ferroelectric Hafnium Oxide Material Enhanced Reliability

Zeppelin (MI 1247/17-1)

Ferroelectric zirconium oxide for piezo- and pyroelectric devices

SoGraphMEM (MI1247/18-1)

Spin Orbit functionalized GRAPHene for resistive-magnetic MEMories

SecuReFET (MI 1247/19-1)

Secure circuits through inherent reconfigurable FET

BioMCross (SL 305/1-1)

Bio inspired Memcomputing via Crossbar Structures

ReLoFEMRis (SL 305 /2-1)

Reconfigurable logic and multi-bit in-memory processing with ferroelectric memristors

FeDiBiS (SL 305/3-1)

Polarization Switching Kinetics in Ferroelectric/Dielectric Bi-Layer Structures

WUMM (MI1247/24-1)

Wurtzite Solid Solutions as a New Material Class for Ferroelectric Microelectronics

EFFSIL300 (100316972)

Efficient and safe power transistors based on 300 mm wafers

F-GaN (100336682)

Development of a reliable and robust foundry process technology for GaN devices based on 200 mm epitaxial GaN on silicon wafers

FreiGaN (100356328)

Development of free-standing GaN wafers with improved homogeneous properties

GaNHoch-VFT (100364091)

Equipment GaN on GaN high voltage and high frequency transistors development

NaMLab Goes Virtual

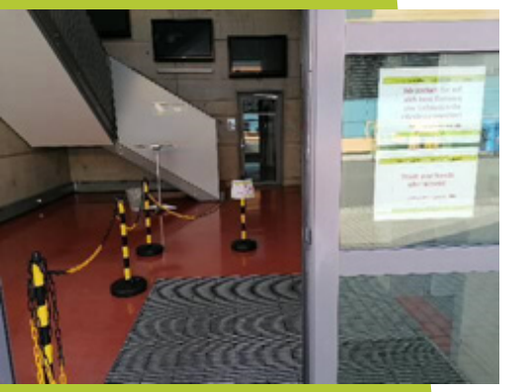


Fig. 1: Redesigned entrance area of NaMLab gGmbH in compliance with hygiene rules during the pandemic crisis of COVID-19.

Fig. 2: During the first lockdown during the COVID-19 crisis, NaMLab gGmbH donated coats, overshoes, and gloves that were missing from the Dresden Municipal Hospitals.

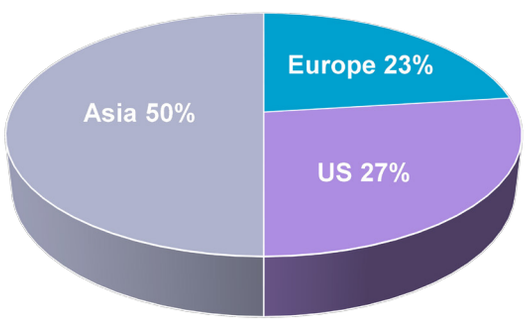


Fig. 3: Origin of participants in the virtual IMW conference by continent.

During the first lockdown due to the COVID-19 pandemic crisis in 2020, NaMLab had to come up with hygiene rules and a reorganization of daily work at short notice. At that time, work in the cleanroom and laboratories could continue according to the established hygiene rules. All scientific office work was moved to the home office. Personal contacts between scientists had to be drastically reduced. Internal meetings, discussions and exchange of know-how were organized online through virtual conferences. International and national conferences and workshops were held online via the Internet. As an example from this challenging time, organized by Dresden-concept e.V., NaMLab handed over several boxes of protective coats, overshoes and gloves, which were not needed at that time, as a donation to the Municipal Hospital Dresden to meet the temporary shortages of protective clothing for their employees. As the pandemic crises progressed, hygiene rules had to be adapted. Following the increasing knowledge about the virus, step by step at least parts of the daily scientific office work could be transferred back to the NaMLab building. But at the end of 2021 still, a significant portion of information exchange was done online.

In 2020 and 2021, NaMLab's efforts to make scientific research on nano-electronic materials, devices and applications more accessible to the general public were hampered by the pandemic crises and the hygiene regulations that were introduced. The only remaining effort was that NaMLab researchers continued to participate as supervisors of the 7th and 8th grade annual internship at the Martin-Andersen-Nexö-Oberschule Dresden. Other joint activities such as the "Long Night of Science", the summer school "Dresden Microelectronics Academy" and the "University Day" of the Technical University Dresden were cancelled or postponed, or NaMLab did not participate.

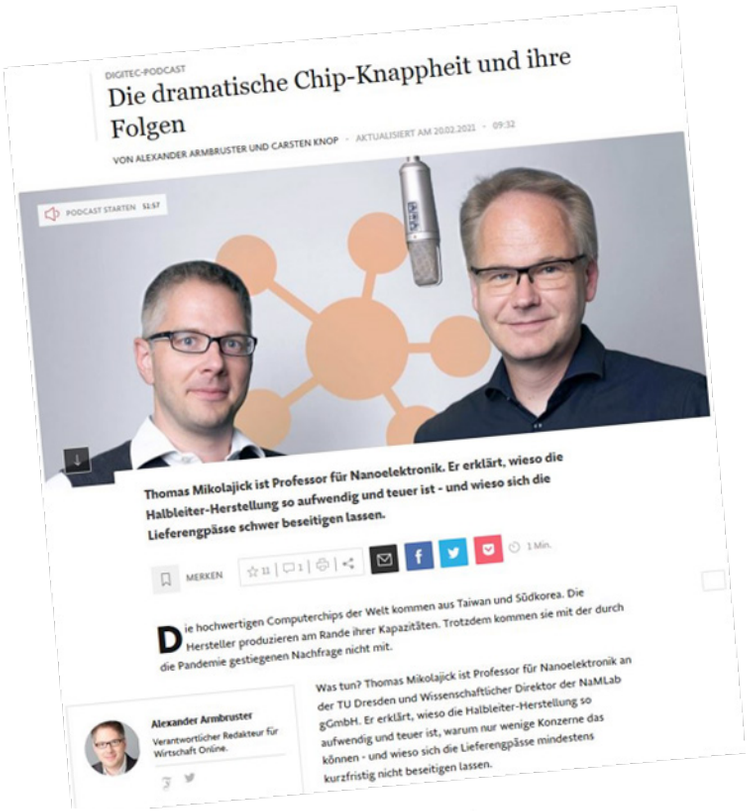
International Memory Workshop 2020/2021

The 2020 edition of the International Memory Workshop (IMW) was planned in Dresden, with NaMLab being one of the local organizers. Due to the COVIC-19 pandemic, the event had to be changed to an online event. A restart as a face-to-face event in Dresden in 2021 was also not possible due to the pandemic crises. The workshop was again held virtually, with about half of the participants from Asia and the rest from Europe and the USA. It is planned to hold the 2022 workshop combined in Dresden and virtually.

Novel High-k Application Workshop 2020/2021

Due to the rapid development of the pandemic crisis in the spring of 2020, the Novel High-k Application Workshop had to be canceled for that year. In May 2021, NaMLab hosted the Novel High-k Application Workshop as a virtual conference held on six consecutive Fridays. This format was well received. More than 80 participants from industry, research institutes, and universities discussed new challenges arising from the application of high-k dielectric materials in micro- and nanoelectron-ics. For 2022, the workshop is planned as a combined virtual and onsite event.

NaMLab In The Media



DIGITEC-PODCAST

Die dramatische Chip-Knappheit und ihre Folgen

VON ALEXANDER ARMBRUSTER UND CARSTEN KNOP - AKTUALISIERT AM 20.02.2021 - 09:32

PODCAST STARTEN 51:57

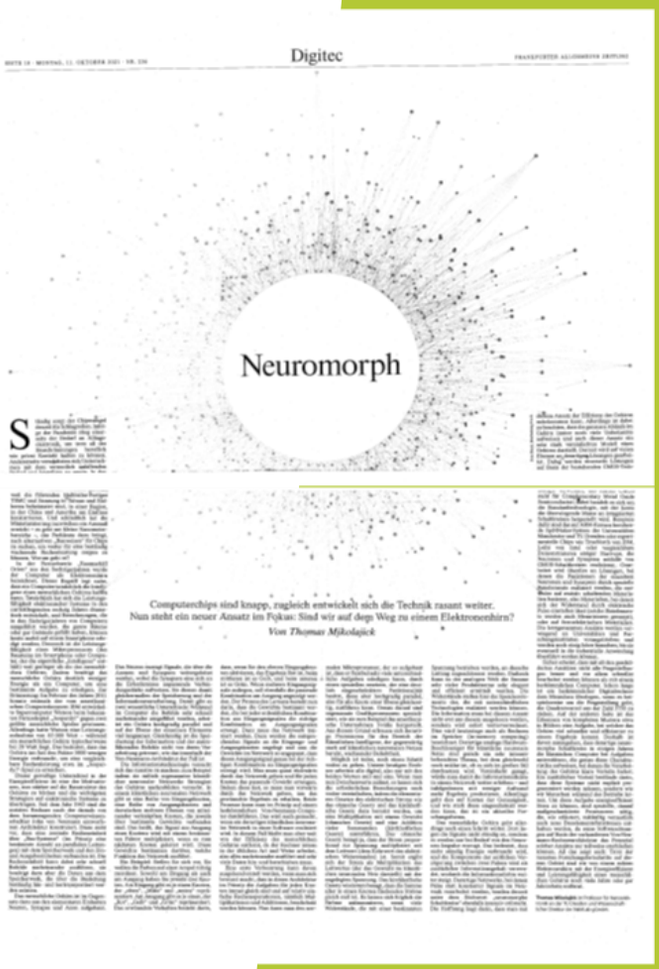
Thomas Mikolajick ist Professor für Nanoelektronik. Er erklärt, wieso die Halbleiter-Herstellung so aufwendig und teuer ist - und wieso sich die Lieferengpässe schwer beseitigen lassen.

MERKEN 1 Min.

Die hochwertigen Computerchips der Welt kommen aus Taiwan und Südkorea. Die Hersteller produzieren am Rande ihrer Kapazitäten. Trotzdem kommen sie mit der durch die Pandemie gestiegenen Nachfrage nicht mit.

Alexander Armbruster
Verantwortlicher Redakteur für Wirtschaft Online.

Was tun? Thomas Mikolajick ist Professor für Nanoelektronik an der TU Dresden und Wissenschaftlicher Direktor der NaMLab gGmbH. Er erklärt, wieso die Halbleiter-Herstellung so aufwendig und teuer ist, warum nur wenige Konzerne das können - und wieso sich die Lieferengpässe mindestens kurzfristig nicht beseitigen lassen.



Digitec

Neuromorph

Computerchips sind knapp, zugleich entwickelt sich die Technik rasant weiter. Nun steht ein neuer Ansatz im Fokus: Sind wir auf dem Weg zu einem Elektronenhirn?

Von Thomas Mikolajick

namlab

CIRROSTRATO

Press Release

Reconfigurable transistors for trustworthy electronics

Dresden, Germany, April 13, 2021 – The *Nanoelectronics Materials Laboratory* (NaMLab gGmbH) has launched the joint research project 'CirroStrato' together with *GLOBALFOUNDRIES Dresden Module One*, *Technical University Dresden*, and *University Bremen* on the use of reconfigurable transistors for the protection of circuit design intellectual property. The project is part of the initiative 'Trustworthy electronics' of the *German Federal Ministry of Education and Research* (BMBF), has a volume of 2.11 M€, and is running for three years.

Our society today is critically dependent on trust in electronic systems. In this regard theft and unauthorized replication of integrated circuits represent a growing problem. Reconfigurable field effect transistors (RFET) embody a nanotechnological solution for protecting electronic components. Circuits made from this new type of transistor make it possible to change the mode of operation dynamically without having to change the underlying physical structure. The actual function remains hidden and cannot be derived by third parties based on the layout. Dr. Trommer, who leads NaMLab's emerging device activities points out: "We aim that security solutions based on RFETs will contribute to Germany's future technology sovereignty".

In addition to the design and demonstration of secure RFET circuit blocks in hardware, an automated design environment (EDA) and algorithms for the optimal placement of these security cells in any integrated circuits will be developed. The resulting circuits will be verified and tested with formal methods with regard to their protective function against typical attack patterns (e.g. SAT attack).

This project has received funding from the *German Federal Ministry of Education and Research* (BMBF). More information can be found on the project webpage of the ministry:

https://www.elektronikforschung.de/projekte/ve-cirrostrato

The joint undertaking will be introduced at the digital conference 'Vertrauenswürdige Elektronik' hosted by the BMBF at 14th of April.

https://www.elektronikforschung.de/vertrauenswuerdigkeit/konferenz

PRESS RELEASE

EU Funds €4M Project to Develop an Extremely Power Efficient Ferrosynaptic Computing Technology

BeFerroSynaptic

Logo of the BeFerroSynaptic project

The amount of data that is being generated in today's electronic devices, and exchanged over communication networks is rapidly increasing. While this is required to unleash the full potential of applications such as image and speech recognition, signal processing for smart sensors and autonomous driving, medical diagnosis from symptoms and scans, handling such a huge amount of data requires novel computing strategies. So far, the most advanced computing algorithms are still mostly executed on traditional large power-hungry computing platforms. The problem, however, is that many small-scale devices, such as smartphones, simply don't have the compute power, energy budget size and complexity that would be required for many tasks. For this reason, applications such as virtual assistants (e.g. Apple's Siri) typically upload speech to the cloud for processing. A strongly growing use of cloud services is expected in near future, resulting in a tremendous increase of energy consumption up to thousands of TWh for data transmission, corresponding to tens of billion tons of CO_2 emission. In fact, the transfer of these large amounts of data to cloud-based systems takes a large amount of energy in itself.

DNN+ Kostenlos bis 12:16 Uhr

11:16 Uhr / 29.01.2020

„Beitrag zur Energiewende": Wie Dresdens Rolle als Lieferant von Leistungselektronik wächst

Dresdens Rolle als Lieferant von Leistungselektronik für E-Autos und Solaranlagen wird in Zukunft wachsen, meint der Nanoelektronik-Professor Thomas Mikolajick. Weitere Branchenvertreter stimmen ihm zu.

„Nachfrage nach Leistungselektronik wird langfristig weiter wachsen"

Diese Leistungshalbleiter auf Galliumnitrid-Basis „können bei hohen Spannungen mit sehr schnellen Schaltfrequenzen betrieben werden", erklärte Thomas Mikolajick. „Damit lassen sich sehr effiziente und kompakte Spannungswandler realisieren. Deren Einsatzgebiete und Absatzmärkte sind vielseitig und stark wachsend, beispielsweise im Bereich der Spannungsversorgung von Serverfarmen in Datenzentren, der Elektromobilität oder der Photovoltaik." Und der Bedarf steige weltweit.

Das sieht man bei Infineon ganz ähnlich: „Die Nachfrage nach Leistungselektronik wird langfristig weiter wachsen", schätzte Standortsprecher Christoph Schumacher ein. Die hiesigen Infineon-Manager erwägen daher, ein viertes Fabrikmodul in Dresden zu bauen, um mehr Leistungs-Halbleiter herstellen zu können. Letztlich muss darüber aber die Konzernspitze entscheiden.

Various press articles about research at NaMLab

Contact: Prof. Dr.-Ing. Thomas Mikolajick

Publication List 2020/2021

Journal Papers 2020-2021

J1	R. Alcala et al., “Influence of oxygen source on the ferroelectric properties of ALD grown Hf1-xZrxO2 films,” J. Phys. D: Appl. Phys., vol. 54, no. 3, p. 035102, Oct. 2020, doi: 10.1088/1361-6463/abbc98.
J2	A. Baasner et al., “The Role of Balancing Nanostructured Silicon Anodes and NMC Cathodes in Lithium-Ion Full-Cells with High Volumetric Energy Density,” J. Electrochem. Soc., vol. 167, no. 2, p. 020516, Jan. 2020, doi: 10.1149/1945-7111/ab68d7.
J3	K. Berggren et al., “Roadmap on emerging hardware and technology for machine learning,” Nanotechnology, vol. 32, no. 1, p. 012002, Oct. 2020, doi: 10.1088/1361-6528/aba70f.
J4	E. T. Breyer et al., “Compact FeFET circuit building blocks for fast and efficient nonvolatile Logic-in-Memory,” IEEE Journal of the Electron Devices Society, pp. 1–1, 2020, doi: 10.1109/JEDS.2020.2987084.
J5	A. Calzolaro et al,, “Material investigations for improving stability of Au free Ta/Al-based ohmic contacts annealed at low temperature for AlGaN/GaN heterostructures,” Semicond. Sci. Technol., vol. 35, no. 7, p. 075011, Jun. 2020, doi: 10.1088/1361-6641/ab8755.
J6	F. Fuchs et al., “Formation and crystallographic orientation of NiSi2–Si interfaces,” Journal of Applied Physics, vol. 128, no. 8, p. 085301, Aug. 2020, doi: 10.1063/1.5143122.
J7	W. Hamouda et al., “Interface chemistry of pristine TiN/La: Hf 0.5 Zr 0.5 O 2 capacitors,” Appl. Phys. Lett., vol. 116, no. 25, p. 252903, Jun. 2020, doi: 10.1063/5.0012595.
J8	W. Hamouda et al., “Physical chemistry of the TiN/Hf0.5Zr0.5O2 interface,” Journal of Applied Physics, vol. 127, no. 6, p. 064105, Feb. 2020, doi: 10.1063/1.5128502.
J9	M. Hoffmann and T. Mikolajick, “Verborgene Energielandschaften,” Physik in unserer Zeit, vol. 51, no. 4, pp. 176–182, 2020, doi: 10.1002/piuz.202001573.
J10	M. Hoffmann, et al., “What’s next for negative capacitance electronics?,” Nat Electron, vol. 3, no. 9, pp. 504–506, Sep. 2020, doi: 10.1038/s41928-020-00474-9.
J11	M. Hyuk Park et al., “Review of Defect Chemistry in Fluorite-structure Ferroelectrics for future electronic devices,” Journal of Materials Chemistry C, 2020, doi: 10.1039/D0TC01695K.
J12	A. Krause et al., “Surface related differences between uncoated versus carbon-coated silicon nanowire electrodes on performance in lithium ion batteries,” Journal of Energy Storage, vol. 27, p. 101052, Feb. 2020, doi: 10.1016/j.est.2019.101052.
J13	L. Krückeberg et al., “Quantum and transport lifetimes in optically induced GaN/AlGaN 2DEGs grown on bulk GaN,” Journal of Vacuum Science & Technology B, vol. NAMBE2019, no. 1, p. 042203, Jun. 2020, doi: 10.1116/1.5145198@jvb.2020.NAMBE2019.issue-1.
J14	U. Langklotz, et al., “Scalable fabrication of gold nanoparticles with adjustable size distribution as catalytic nuclei for the CVD growth of silicon nanowires,” Appl. Surf. Sci., vol. 502, p. 144203, 2020, doi: 10.1016/j.apsusc.2019.144203.
J15	S. Li, et al., “Involvement of Unsaturated Switching in the Endurance Cycling of Si-doped HfO2 Ferroelectric Thin Films,” Advanced Electronic Materials, vol. 6, no. 8, p. 2000264, 2020, doi: 10.1002/aelm.202000264.
J16	P. D. Lomenzo et al., “Universal Curie constant and pyroelectricity in doped ferroelectric HfO2 thin films,” Nano Energy, vol. 74, p. 104733, Aug. 2020, doi: 10.1016/j.nanoen.2020.104733.
J17	P. D. Lomenzo, et al., “A Gibbs energy view of double hysteresis in ZrO2 and Si-doped HfO2,” Appl. Phys. Lett., vol. 117, no. 14, p. 142904, Oct. 2020, doi: 10.1063/5.0018199.
J18	P. D. Lomenzo, et al., “Depolarization as Driving Force in Antiferroelectric Hafnia and Ferroelectric Wake-Up,” ACS Appl. Electron. Mater., vol. 2, no. 6, pp. 1583–1595, Jun. 2020, doi: 10.1021/acsaelm.0c00184.
J19	M. Materano et al., “Polarization switching in thin doped HfO2 ferroelectric layers,” Appl. Phys. Lett., vol. 117, no. 26, p. 262904, Dec. 2020, doi: 10.1063/5.0035100.
J20	M. Materano et al., “Influence of Oxygen Content on the Structure and Reliability of Ferroelectric HfxZr1–xO2 Layers,” ACS Appl. Electron. Mater., vol. 2, no. 11, pp. 3618–3626, Nov. 2020, doi: 10.1021/acsaelm.0c00680.
J21	T. Mauersberger, et al., “Size effect of electronic properties in highly arsenic-doped silicon nanowires,” Solid-State Electronics, vol. 168, p. 107724, Jun. 2020, doi: 10.1016/j.sse.2019.107724.

J22	B. Max, et al., “Built-in bias fields for retention stabilisation in hafnia-based ferroelectric tunnel junctions,” Electronics Letters, vol. 56, no. 21, pp. 1108–1110, Sep. 2020, doi: 10.1049/el.2020.1529.
J23	B. Max, et al., “Hafnia-Based Double-Layer Ferroelectric Tunnel Junctions as Artificial Synapses for Neuromorphic Computing,” ACS Appl. Electron. Mater., vol. 2, no. 12, pp. 4023–4033, Dec. 2020, doi: 10.1021/acsaelm.0c00832.
J24	F. Mehmood, et al., “Lanthanum doping induced structural changes and their implications on ferroelectric properties of Hf1−xZrxO2 thin film,” Appl. Phys. Lett., vol. 117, no. 9, p. 092902, Aug. 2020, doi: 10.1063/5.0021007.
J25	T. Mikolajick, et al., “The Past, the Present, and the Future of Ferroelectric Memories,” IEEE Transactions on Electron Devices, vol. 67, no. 4, pp. 1434–1443, Apr. 2020, doi: 10.1109/TED.2020.2976148.
J26	H. Mulaosmanovic, et al., “Reconfigurable frequency multiplication with a ferroelectric transistor,” Nat Electron, vol. 3, no. 7, pp. 391–397, Jul. 2020, doi: 10.1038/s41928-020-0413-0.
J27	H. Mulaosmanovic et al., “Impact of Read Operation on the Performance of HfO2-Based Ferroelectric FETs,” IEEE Electron Device Letters, vol. 41, no. 9, pp. 1420–1423, Sep. 2020, doi: 10.1109/LED.2020.3007220.
J28	H. Mulaosmanovic et al., “Frequency Mixing with HfO2-Based Ferroelectric Transistors,” ACS Appl. Mater. Interfaces, vol. 12, no. 40, pp. 44919–44925, Oct. 2020, doi: 10.1021/acsami.0c11155.
J29	H. Mulaosmanovic et al., “Investigation of Accumulative Switching in Ferroelectric FETs: Enabling Universal Modeling of the Switching Behavior,” IEEE Transactions on Electron Devices, vol. 67, no. 12, pp. 5804–5809, Dec. 2020, doi: 10.1109/TED.2020.3031249.
J30	H. Mulaosmanovic et al., “Interplay Between Switching and Retention in HfO2-Based Ferroelectric FETs,” IEEE Transactions on Electron Devices, vol. 67, no. 8, pp. 3466–3471, Aug. 2020, doi: 10.1109/TED.2020.3004033.
J31	S. J. Park et al., “Channel Length-Dependent Operation of Ambipolar Schottky-Barrier Transistors on a Single Si Nanowire,” ACS Appl. Mater. Interfaces, vol. 12, no. 39, pp. 43927–43932, Sep. 2020, doi: 10.1021/acsami.0c12595.
J32	M. Raitza et al., “Quantitative Characterization of Reconfigurable Transistor Logic Gates,” IEEE Access, vol. 8, pp. 112598–112614, 2020, doi: 10.1109/ACCESS.2020.3001352.
J33	T. Schenk, et al., “Memory Technology – A Primer for Material Scientists,” Rep. Prog. Phys., 2020, doi: 10.1088/1361-6633/ab8f86.
J34	S. Schmult et al., “Normally-Off Operation of Lateral Field-Effect Transistors Fabricated from Ultrapure GaN/AlGaN Heterostructures,” physica status solidi (a), vol. 217, no. 7, p. 1900732, 2020, doi: 10.1002/pssa.201900732.
J35	V. Sessi et al., “A Silicon Nanowire Ferroelectric Field-Effect Transistor,” Advanced Electronic Materials, vol. 6, no. 4, p. 1901244, 2020, doi: 10.1002/aelm.201901244.
J36	M. Simon et al., “Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States,” IEEE Electron Device Letters, vol. 41, no. 7, pp. 1110–1113, Jul. 2020, doi: 10.1109/LED.2020.2997319.
J37	I. Stolichnov et al., “Intrinsic or nucleation-driven switching: An insight from nanoscopic analysis of negative capacitance Hf1−xZrxO2-based structures,” Appl. Phys. Lett., vol. 117, no. 17, p. 172902, Oct. 2020, doi: 10.1063/5.0021272.
J38	T. Szyjka et al., “Enhanced Ferroelectric Polarization in TiN/HfO2/TiN Capacitors by Interface Design,” ACS Appl. Electron. Mater., vol. 2, no. 10, pp. 3152–3159, Oct. 2020, doi: 10.1021/acsaelm.0c00503.
J39	D. Tröger, et al., “Al2O3-TiOx as full area passivating contacts for silicon surfaces utilizing oxygen scavenging titanium interlayers,” Solar Energy Materials and Solar Cells, vol. 215, p. 110651, Sep. 2020, doi: 10.1016/j.solmat.2020.110651.
J40	J. Trommer, et al., “Inherent Charge-Sharing-Free Dynamic Logic Gates Employing Transistors With Multiple Independent Inputs,” IEEE Journal of the Electron Devices Society, vol. 8, pp. 740–747, 2020, doi: 10.1109/JEDS.2020.2986940.

J41	S. Voswinckel, Tet al., “Influence of the active leakage current pathway on the potential induced degradation of CIGS thin film solar modules,” Solar Energy, vol. 197, pp. 455–461, Feb. 2020, doi: 10.1016/j.solener.2019.12.078.
J42	A. Ascoli, et al., “On Local Activity and Edge of Chaos in a NaMLab Memristor,” Frontiers in Neuroscience, vol. 15, p. 233, 2021, doi: 10.3389/fnins.2021.651452.
J43	L. Azevedo Antunes, et al., “An unexplored antipolar phase in HfO2 from first principles and implication for wake-up mechanism,” Appl. Phys. Lett., vol. 119, no. 8, p. 082903, Aug. 2021, doi: 10.1063/5.0063808.
J44	L. Balaghi et al., “High electron mobility in strained GaAs nanowires,” Nat Commun, vol. 12, no. 1, p. 6642, Nov. 2021, doi: 10.1038/s41467-021-27006-z.
J45	L. Baumgarten et al., “Impact of vacancies and impurities on ferroelectricity in PVD- and ALD-grown HfO2 films,” Appl. Phys. Lett., vol. 118, no. 3, p. 032903, Jan. 2021, doi: 10.1063/5.0035686.
J46	E. T. Breyer, et al., “Perspective on ferroelectric, hafnium oxide based transistors for digital beyond von-Neumann computing,” Appl. Phys. Lett., vol. 118, no. 5, p. 050501, Feb. 2021, doi: 10.1063/5.0035281.
J47	A. Calzolaro, et al., “Surface Preconditioning and Postmetallization Anneal Improving Interface Properties and Vth Stability under Positive Gate Bias Stress in AlGaN/GaN MIS-HEMTs “,Phys. Status Solidi A 2021, 218, 2000585; doi 10.1002/pssa.202000585
J48	S. Dutta et al., “Piezoelectricity in hafnia,” Nat Commun, vol. 12, no. 1, p. 7301, Dec. 2021, doi: 10.1038/s41467-021-27480-5.
J49	T. Francois et al., “Impact of area scaling on the ferroelectric properties of back-end of line compatible Hf0.5Zr0.5O2 and Si:HfO2-based MFM capacitors,” Appl. Phys. Lett., vol. 118, no. 6, p. 062904, Feb. 2021, doi: 10.1063/5.0035650.
J50	D. Hiller, et al., “The negative fixed charge of atomic layer deposited aluminium oxide—a two-dimensional SiO2/AlO x interface effect,” J. Phys. D: Appl. Phys., vol. 54, no. 27, p. 275304, Apr. 2021, doi: 10.1088/1361-6463/abf675.
J51	M. Hoffmann et al., “Intrinsic Nature of Negative Capacitance in Multidomain Hf0.5Zr0.5O2-Based Ferroelectric/Dielectric Heterostructures,” Advanced Functional Materials, vol. n/a, no. n/a, p. 2108494, Oct. 2021, doi: 10.1002/adfm.202108494.
J52	M. Hoffmann, S. Slesazeck, and T. Mikolajick, “Progress and future prospects of negative capacitance electronics: A materials perspective,” APL Materials, vol. 9, no. 2, p. 020902, Feb. 2021, doi: 10.1063/5.0032954.
J53	M. Hoffmann et al., “Antiferroelectric negative capacitance from a structural phase transition in zirconia,” arXiv:2104.10811 [cond-mat, physics:physics], Apr. 2021, Accessed: Dec. 20, 2021. [Online]. Available: http://arxiv.org/abs/2104.10811
J54	D.-Y. Jeon, S. J. Park, S. Pregl, T. Mikolajick, and W. M. Weber, “Reconfigurable thin-film transistors based on a parallel array of Si-nanowires,” Journal of Applied Physics, vol. 129, no. 12, p. 124504, Mar. 2021, doi: 10.1063/5.0036029.
J55	M. B. Khan et al., “Controlled Silicidation of Silicon Nanowires Using Flash Lamp Annealing,” Langmuir, vol. 37, no. 49, pp. 14284–14291, Dec. 2021, doi: 10.1021/acs.langmuir.1c01862.
J56	D. Kleimaier et al., “Demonstration of a p-Type Ferroelectric FET With Immediate Read-After-Write Capability,” IEEE Electron Device Letters, vol. 42, no. 12, pp. 1774–1777, Dec. 2021, doi: 10.1109/LED.2021.3118645.
J57	M. Knaut, et al., “Flash-Lamp Enabled Atomic Layer Deposition of Titanium Oxide,” Meet. Abstr., vol. MA2021-02, no. 29, p. 869, Oct. 2021, doi: 10.1149/MA2021-0229869mtgabs.
J58	S. Lancaster et al., “Atomic layer deposition of ferroelectric Hf0.5Zr0.5O2 on single-layer, CVD-grown graphene,” arXiv:2109.09543 [cond-mat, physics:physics], Nov. 2021, Accessed: Dec. 20, 2021. [Online]. Available: http://arxiv.org/abs/2109.09543
J59	D. H. Lee et al., “Domains and domain dynamics in fluorite-structured ferroelectrics,” Applied Physics Reviews, vol. 8, no. 2, p. 021312, Jun. 2021, doi: 10.1063/5.0047977.
J60	S. Li, et al., “Temperature-Dependent Subcycling Behavior of Si-Doped HfO2 Ferroelectric Thin Films,” ACS Appl. Electron. Mater., vol. 3, no. 5, pp. 2415–2422, May 2021, doi: 10.1021/acsaelm.1c00330.
J61	P. D. Lomenzo, et al., “Pyroelectric dependence of atomic layer-deposited Hf0.5Zr0.5O2 on film thickness and annealing temperature,” Appl. Phys. Lett., vol. 119, no. 11, p. 112903, Sep. 2021, doi: 10.1063/5.0062789.

J62	P. D. Lomenzo et al., “Harnessing Phase Transitions in Antiferroelectric ZrO2 Using the Size Effect,” Advanced Electronic Materials, vol. n/a, no. n/a, p. 2100556, Oct. 2021, doi: 10.1002/aelm.202100556.
J63	P. D. Lomenzo, et al., “(Invited) Ferroelectric Hafnium Oxide for Non-Volatile Memory Applications: From Single Capacitors to Memory Arrays,” Meet. Abstr., vol. MA2021-02, no. 12, p. 611, Oct. 2021, doi: 10.1149/MA2021-0212611mtgabs.
J64	M. Materano, et al., “Interplay between oxygen defects and dopants: effect on structure and performance of HfO2-based ferroelectrics,” Inorganic Chemistry Frontiers, vol. 8, no. 10, pp. 2650–2672, 2021, doi: 10.1039/D1QI00167A.
J65	T. Mauersberger et al., “Single-step reactive ion etching process for device integration of hafnium-zirconium-oxide (HZO)/titanium nitride (TiN) stacks,” Semicond. Sci. Technol., vol. 36, no. 9, p. 095025, Aug. 2021, doi: 10.1088/1361-6641/ac1827.
J66	T. Mikolajick et al., “20 Years of reconfigurable field-effect transistors: From concepts to future applications,” Solid-State Electronics, vol. 186, p. 108036, Dec. 2021, doi: 10.1016/j.sse.2021.108036.
J67	T. Mikolajick et al., “Next generation ferroelectric materials for semiconductor process integration and their applications,” Journal of Applied Physics, vol. 129, no. 10, p. 100901, Mar. 2021, doi: 10.1063/5.0037617.
J68	T. Mikolajick and U. Schroeder, “Ferroelectricity in bulk hafnia,” Nat. Mater., vol. 20, no. 6, pp. 718–719, Jun. 2021, doi: 10.1038/s41563-020-00914-z.
J69	T. Mikolajick, et al., “Special topic on ferroelectricity in hafnium oxide: Materials and devices,” Appl. Phys. Lett., vol. 118, no. 18, p. 180402, May 2021, doi: 10.1063/5.0054064.
J70	T. Mittmann et al., “Stabilizing the ferroelectric phase in HfO2 -based films sputtered from ceramic targets under ambient oxygen,” Nanoscale, vol. 13, no. 2, pp. 912–921, 2021, doi: 10.1039/D0NR07699F.
J71	T. Mittmann et al., “Impact of Iridium Oxide Electrodes on the Ferroelectric Phase of Thin Hf0.5Zr0.5O2 Films,” physica status solidi (RRL) – Rapid Research Letters, vol. 15, no. 5, p. 2100012, 2021, doi: 10.1002/pssr.202100012.
J72	H. Mulaosmanovic, et al., “Ferroelectric field-effect transistors based on HfO2: a review,” Nanotechnology, vol. 32, no. 50, p. 502002, Sep. 2021, doi: 10.1088/1361-6528/ac189f.
J73	H. Mulaosmanovic et al., “Effect of the Si Doping Content in HfO2 Film on the Key Performance Metrics of Ferroelectric FETs,” IEEE Transactions on Electron Devices, vol. 68, no. 9, pp. 4773–4779, Sep. 2021, doi: 10.1109/TED.2021.3100005.
J74	H. Mulaosmanovic, et al., “Ferroelectric transistors with asymmetric double gate for memory window exceeding 12 V and disturb-free read,” Nanoscale, vol. 13, no. 38, pp. 16258–16266, 2021, doi: 10.1039/D1NR05107E.
J75	J. Okuno et al., “1T1C FeRAM memory array based on ferroelectric HZO with capacitor under bitline,” IEEE Journal of the Electron Devices Society, pp. 1–1, 2021, doi: 10.1109/JEDS.2021.3129279.
J76	M. H. Park, et al., “Binary ferroelectric oxides for future computing paradigms,” MRS Bulletin, Dec. 2021, doi: 10.1557/s43577-021-00210-4.
J77	T. V. Perevalov et al., “Bipolar conductivity in ferroelectric La:HfZrO films,” Appl. Phys. Lett., vol. 118, no. 26, p. 262903, Jun. 2021, doi: 10.1063/5.0050748.
J78	T. V. Perevalov et al., “The atomic and electronic structure of Hf0.5Zr0.5O2 and Hf0.5Zr0.5O2:La films,” Journal of Science: Advanced Materials and Devices, vol. 6, no. 4, pp. 595–600, Dec. 2021, doi: 10.1016/j.jsamd.2021.08.001.
J79	C. Roemer et al., “Physics-Based DC Compact Modeling of Schottky Barrier and Reconfigurable Field-Effect Transistors,” IEEE Journal of the Electron Devices Society, pp. 1–1, 2021, doi: 10.1109/JEDS.2021.3136981.
J80	M. Simon et al., “Lateral Extensions to Nanowires for Controlling Nickel Silicidation Kinetics: Improving Contact Uniformity of Nanoelectronic Devices,” ACS Appl. Nano Mater., vol. 4, no. 5, pp. 4371–4378, May 2021, doi: 10.1021/acsanm.0c03072.
J81	V. V. Solovyev, et al., “Light-tunable 2D subband population in a GaN/AlGaN heterostructure,” Appl. Phys. Lett., vol. 118, no. 1, p. 013101, Jan. 2021, doi: 10.1063/5.0027010.
J82	B. Sun et al., “On the Operation Modes of Dual-Gate Reconfigurable Nanowire Transistors,” IEEE Transactions on Electron Devices, vol. 68, no. 7, pp. 3684–3689, Jul. 2021, doi: 10.1109/TED.2021.3081527.

Journal Papers 2020-2021

J83	T. Szyjka et al., “Chemical Stability of IrO2 Top Electrodes in Ferroelectric Hf0.5Zr0.5O2-Based Metal–Insulator–Metal Structures: The Impact of Annealing Gas,” physica status solidi (RRL) – Rapid Research Letters, vol. 15, no. 5, p. 2100027, 2021, doi: 10.1002/pssr.202100027.
J84	D. Tröger, et al., “Hole selective nickel oxide as transparent conductive oxide,” J. Vac. Sci. Technol. A, vol. 40, no. 1, p. 013409, 2021, doi: 10.1116/6.0001391.
J85	M. Weiher, et al., “Improved Vertex Coloring With NbO_x Memristor-Based Oscillatory Networks,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 5, pp. 2082–2095, May 2021, doi: 10.1109/TCSI.2021.3061973.
J86	C. Weimer,et al., “Pulsed Measurements Based Investigation of Trap Capture and Emission Processes in CNTFETs,” IEEE Transactions on Nanotechnology, vol. 20, pp. 459–465, 2021, doi: 10.1109/TNANO.2021.3080455.

Conference Proceedings 2020-2021

C1	E. T. Breyer, et al., “Flexible Memory, Bit-Passing and Mixed Logic/Memory Operation of two Intercoupled FeFET Arrays,” in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020, pp. 1–5. doi: 10.1109/ISCAS45731.2020.9181279.
C2	T. Chohan, et al., “SOTF-BTI - an S-Parameters based on-the-fly Bias Temperature Instability Characterization Method,” in 2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Jul. 2020, pp. 1–5. doi: 10.1109/IPFA49335.2020.9260732.
C3	L. Grenouillet et al., “Nanosecond Laser Anneal (NLA) for Si-Implanted HfO2 Ferroelectric Memories Integrated in Back-End of Line (BEOL),” in 2020 IEEE Symposium on VLSI Technology, Jun. 2020, pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265061.
C4	M. Hoffmann, et al., “Experimental Ferroelectric Energy Landscapes: Insights into the Origin of Negative Capacitance,” in 2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF), Jul. 2020, pp. 1–2. doi: 10.1109/IFCS-ISAF41089.2020.9234897.
C5	M. B. Khan et al., “Towards Scalable Reconfigurable Field Effect Transistor using Flash Lamp Annealing,” in 2020 Device Research Conference (DRC), Jun. 2020, pp. 1–2. doi: 10.1109/DRC50226.2020.9135146.
C6	P. D. Lomenzo et al., “AFE-like Hysteresis Loops from Doped HfO2: Field Induced Phase Changes and Depolarization Fields,” in 2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF), Jul. 2020, pp. 1–4. doi: 10.1109/IFCS-ISAF41089.2020.9234872.
C7	P. D. Lomenzo, et al., “Thickness Scaling of AFE-RAM ZrO2 Capacitors with High Cycling Endurance and Low Process Temperature,” in 2020 IEEE International Memory Workshop (IMW), May 2020, pp. 1–4. doi: 10.1109/IMW48823.2020.9108146.
C8	C. Maneux et al., Eds., “Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence”. 67th IEEE International Electron Devices Meeting 2021.
C9	F. Mehmood, et al., “Reliability improvement of ferroelectric Hf0.5Zr0.5O2 thin films by Lanthanum doping for FeRAM applications,” in 2020 Device Research Conference (DRC), Jun. 2020, pp. 1–2. doi: 10.1109/DRC50226.2020.9150531.
C10	T. Mikolajick, et al., “Hafnium oxide as an enabler for competitive ferroelectric devices,” in 2020 IEEE Silicon Nanoelectronics Workshop (SNW), Jun. 2020, pp. 1–2. doi: 10.1109/SNW50361.2020.9131618.
C11	T. Mittmann, et al., “Impact of Oxygen Vacancy Content in Ferroelectric HZO films on the Device Performance,” in 2020 IEEE International Electron Devices Meeting (IEDM), Dec. 2020, pp. 18.4.1-18.4.4. doi: 10.1109/IEDM13553.2020.9372097.
C12	H. Mulaosmanovic, et al., “Switching and Charge Trapping in HfO2-based Ferroelectric FETs: An Overview and Potential Applications,” in 2020 4th IEEE Electron Devices Technology Manufacturing Conference (EDTM), Apr. 2020, pp. 1–4. doi: 10.1109/EDTM47692.2020.9118005.
C13	H. Mulaosmanovic et al., “HfO2-based ferroelectric FETs: Performance of single devices and mini-arrays,” in 2020 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Aug. 2020, pp. 146–147. doi: 10.1109/VLSI-TSA48913.2020.9203615.

Conference Proceedings 2020-2021

C14	J. Okuno et al., "SoC Compatible 1T1C FeRAM Memory Array Based on Ferroelectric Hf0.5Zr0.5O2," in 2020 IEEE Symposium on VLSI Technology, Jun. 2020, pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265063.
C15	T. Xie et al., "Investigation of HVPE grown layers on MOVPE GaN/sapphire templates for application as drift layer in vertical GaN power devices," in 2020 13th International Conference on Advanced Semiconductor Devices And Microsystems (ASDAM), Oct. 2020, pp. 135–138. doi: 10.1109/ASDAM50306.2020.9393849.
C16	H. Zhou et al., "Application and Benefits of Target Programming Algorithms for Ferroelectric HfO2 Transistors," in 2020 IEEE International Electron Devices Meeting (IEDM), Dec. 2020, pp. 18.6.1-18.6.4. doi: 10.1109/IEDM13553.2020.9371975.
C17	H. Zhou et al., "Endurance and targeted programming behavior of HfO2-FeFETs," in 2020 IEEE International Memory Workshop (IMW), May 2020, pp. 1–4. doi: 10.1109/IMW48823.2020.9108131.
C18	A. Ascoli, et al., "Control Strategies to Optimize Graph Coloring via M-CNNs with Locally-Active NbOx Memristors," in 2021 10th International Conference on Modern Circuits and Systems Technologies (MOCAST), Jul. 2021, pp. 1–8. doi: 10.1109/MOCAST52088.2021.9493418.
C19	A. Calzolaro, et al., "Integration and Reliability Aspects of Low-Temperature and Au-free Ta/Al-based Ohmic Contacts for AlGaN/GaN MIS-HEMTs," in ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC), Sep. 2021, pp. 307–310. doi: 10.1109/ESSDERC53440.2021.9631788.
C20	E. Covi et al., "Ferroelectric Tunneling Junctions for Edge Computing," in 2021 IEEE International Symposium on Circuits and Systems (ISCAS), May 2021, pp. 1–5. doi: 10.1109/ISCAS51556.2021.9401800.
C21	R. Fontanini et al., "Polarization switching and interface charges in BEOL compatible Ferroelectric Tunnel Junctions," in ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC), Sep. 2021, pp. 255–258. doi: 10.1109/ESSDERC53440.2021.9631812.
C22	T. Francois et al., "16kbit HfO2:Si-based 1T-1C FeRAM Arrays Demonstrating High Performance Operation and Solder Reflow Compatibility," in 2021 IEEE International Electron Devices Meeting (IEDM), Dec. 2021, pp. 33.1.1-33.1.4. doi: 10.1109/IEDM19574.2021.9720640.
C23	P. D. Lomenzo, et al., "Electronic Contributions to Ferroelectricity and Field-Induced Phase Transitions in Doped-HfO2," in 2021 IEEE International Symposium on Applications of Ferroelectrics (ISAF), May 2021, pp. 1–4. doi: 10.1109/ISAF51943.2021.9477323.
C24	C. Maneux et al., "Why neuromorphic computing need novel 3D technologies? A view from FVLLMONTI European project consortium (Invited)," presented at the High Performance Embedded Architecture and Compilation, Computing Systems Week, (HiPEAC CSW) Autumn 2021, Oct. 2021. Accessed: Dec. 20, 2021. [Online]. Available: https://hal.archives-ouvertes.fr/hal-03408071
C25	C. Marchand, et al., "FeFET based Logic-in-Memory: an overview," in 2021 16th International Conference on Design Technology of Integrated Systems in Nanoscale Era (DTIS), Jun. 2021, pp. 1–6. doi: 10.1109/DTIS53253.2021.9505078.
C26	T. Mikolajick, et al., "Optimization and Application of Niobium Oxide based Memristive NDR devices," in 2021 17th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA), Sep. 2021, pp. 1–4. doi: 10.1109/CNNA49188.2021.9610782.
C27	T. Mikolajick, et al., "The Case for Ferroelectrics in Future Memory Devices," in 2021 5th IEEE Electron Devices Technology Manufacturing Conference (EDTM), Apr. 2021, pp. 1–3. doi: 10.1109/EDTM50988.2021.9420821.
C28	H. Mulaosmanovic, et al., "Reliability aspects of ferroelectric hafnium oxide for application in non-volatile memories," in 2021 IEEE International Reliability Physics Symposium (IRPS), Mar. 2021, pp. 1–6. doi: 10.1109/IRPS46558.2021.9405215.
C29	I. O'Connor et al., "Analysis of Energy-Delay-Product of a 3D Vertical Nanowire FET Technology," in 2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS), Sep. 2021, pp. 1–4. doi: 10.1109/EuroSOI-ULIS53016.2021.9560180.
C30	J. Okuno et al., "Demonstration of 1T1C FeRAM Arrays for Nonvolatile Memory Applications," in 2021 20th International Workshop on Junction Technology (IWJT), Jun. 2021, pp. 1–4. doi: 10.23919/IWJT52818.2021.9609497.
C31	J. Okuno et al., "High-Endurance and Low-Voltage operation of 1T1C FeRAM Arrays for Nonvolatile Memory Application," in 2021 IEEE International Memory Workshop (IMW), May 2021, pp. 1–3. doi: 10.1109/IMW51353.2021.9439595.

Conference Proceedings 2020-2021

C32	I. Polian et al., “Nano Security: From Nano-Electronics to Secure Systems,” in 2021 Design, Automation Test in Europe Conference Exhibition (DATE), Feb. 2021, pp. 1334–1339. doi: 10.23919/DATE51398.2021.9474187.
C33	S. Rai et al., “Perspectives on Emerging Computation-in-Memory Paradigms,” in 2021 Design, Automation Test in Europe Conference Exhibition (DATE), Feb. 2021, pp. 1925–1934. doi: 10.23919/DATE51398.2021.9473976.
C34	C. Roemer et al., “Uniform DC Compact Model for Schottky Barrier and Reconfigurable Field-Effect Transistors,” in 2021 IEEE Latin America Electron Devices Conference (LAEDC), Apr. 2021, pp. 1–4. doi: 10.1109/LAEDC51812.2021.9437954.
C35	V. Sessi et al., “Back-Bias Reconfigurable Field Effect Transistor: A Flexible Add-On Functionality for 22 nm FDSOI,” in 2021 Silicon Nanoelectronics Workshop (SNW), Jun. 2021, pp. 1–2. doi: 10.1109/SNW51795.2021.00005.
C36	F. A. Velarde Gonzalez, et al., “RF small-signal modeling of HCI degradation in FDSOI NMOSFET using BSIM-IMG,” in 2021 IEEE International Integrated Reliability Workshop (IIRW), Oct. 2021, pp. 1–5. doi: 10.1109/IIRW53245.2021.9635622.
C37	H. Zhou et al., “Mechanism of Retention Degradation after Endurance Cycling of HfO2-based Ferroelectric Transistors,” in 2021 Symposium on VLSI Technology, Jun. 2021, pp. 1–2.

Monographs (Book Chapters) 2020-2021

M1	H. Mulaosmanovic, et al., “FeFETs for Neuromorphic Systems,” in Ferroelectric-Gate Field Effect Transistor Memories: Device Physics and Applications, B.-E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S.-M. Yoon, Eds. Singapore: Springer, 2020, pp. 399–411. doi: 10.1007/978-981-15-1212-4_20.
M2	H. Mulaosmanovic, et al., “Switching in Nanoscale Hafnium Oxide-Based Ferroelectric Transistors,” in Ferroelectric-Gate Field Effect Transistor Memories: Device Physics and Applications, B.-E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S.-M. Yoon, Eds. Singapore: Springer, 2020, pp. 97–108. doi: 10.1007/978-981-15-1212-4_5.
M3	S. Spiga, et al., Memristive Devices for Brain-Inspired Computing: From Materials, Devices, and Circuits to Applications - Computational Memory, Deep Learning, and Spiking Neural Networks. Woodhead Publishing, 2020.

Invited Talks 2020-2021

I1	C. Maneux et al., “How novel technologies can boost neuromorphic computing? A view from European project consortia (Invited).” Apr. 2021. Accessed: Apr. 13, 2022. [Online]. Available: https://hal.archives-ouvertes.fr/hal-03408059
I2	Uwe Schroeder, ‘Hafnium oxide: Ferroelectric Hafnium Oxide: From Memory to Emerging Applications’, VLSI Hawaii 2020 now online
I3	Uwe Schroeder, ‘Causes for Ferroelectricity in Doped HfO2 Films - The Tenth Anniversary of the First Publication Announcing Ferroelectricity in Doped HfO2’, ISAF 2021 now online
I4	Uwe Schroeder, ‘Stabilization of the Ferroelectric Phase in Doped Hafnium Oxide Films: Influence of Dopants and Oxygen Vacancies’, IWMP Bucharest 2021, Rumania
I5	Uwe Schroeder, ‘Influence of Dopants and Oxygen Vacancies on the Stabilization of the Ferroelectric Phase in Doped Hafnium Oxide Films’, IU-MRS 2021 Jesu Island Korea now online
I6	P. D. Lomenzo et al., ’Ferroelectric Hafnium Oxide for Non-Volatile Memory Applications: From Single Capacitors to Memory Arrays’, ECS Orlando 2021 now online
I7	Uwe Schroeder, ‘Stabilization and Phase Transitions in Ferroelectric Doped Hafnium Oxide Films: Influence of Dopants and Oxygen Vacancies’, E-MRS Fall 2021 now online
I8	Uwe Schroeder, Halid Mulamanovic, ‘Ferroelectric Doped Hafnium Oxide: From Switching Kinetics to Neuromorphic Elements’, MRS Fall 2021 Boston now online

Invited Talks 2020-2021

I9	U. Schroeder et al. 'Impact of depolarization fields on the ferroelectric switching behavior in doped HfO2', Ferro 2020 Washington
I10	Thomas Mikolajick et al., 'Hafnium oxide as an enabler for competitive ferroelectric devices', Silicon Nanoelectronic Workshop 2020 Hawaii now online
I11	Jens Trommer et al. „ Reconfigurable Field Effect Transistor as a Security Device" Silicon Saxony Day 2021. 27.05.21 Dresden; https://www.silicon-saxony-day.de/highlights/speakers/dr-jens-trommer
I12	Jens Trommer et al. " Neuartige rekonfigurierbare Transistoren für den Know-how-Schutz von Elektronikkomponenten " Digitalen Konferenz „Vertrauenswürdige Elektronik" am 14.04.2021

Education

PhD thesis

P1	M. Simon “Top-down Fabrication of Reconfigurable Nanowire Electronics“, TU Dresden 2021
P2	E. Breyer “Development and Investigation of Novel Logic-in-Memory and Nonvolatile Logic Circuits Utilizing Hafnium Oxide-Based Ferroelectric Field-Effect Transistors”, TU Dresden 2021
P3	M. Hoffmann “Negative Capacitance in Ferroelectric Materials”, TU Dresden 2020
P4	B. Max “Kombination Resistiver und Ferroelektrischer Schaltmechanismen in HfO2-basierten Bauelementen”, TU Dresden 2021
P5	P. Hoffmann, “Investigation of correlations between HVPE growth, crystal properties and dopant incorporation in gallium nitride“, TU Dresden 2020
P6	R. Hentschel, “Vertical Gallium Nitride Power Devices: Fabrication and Characterisation”, TU Dresden 2020

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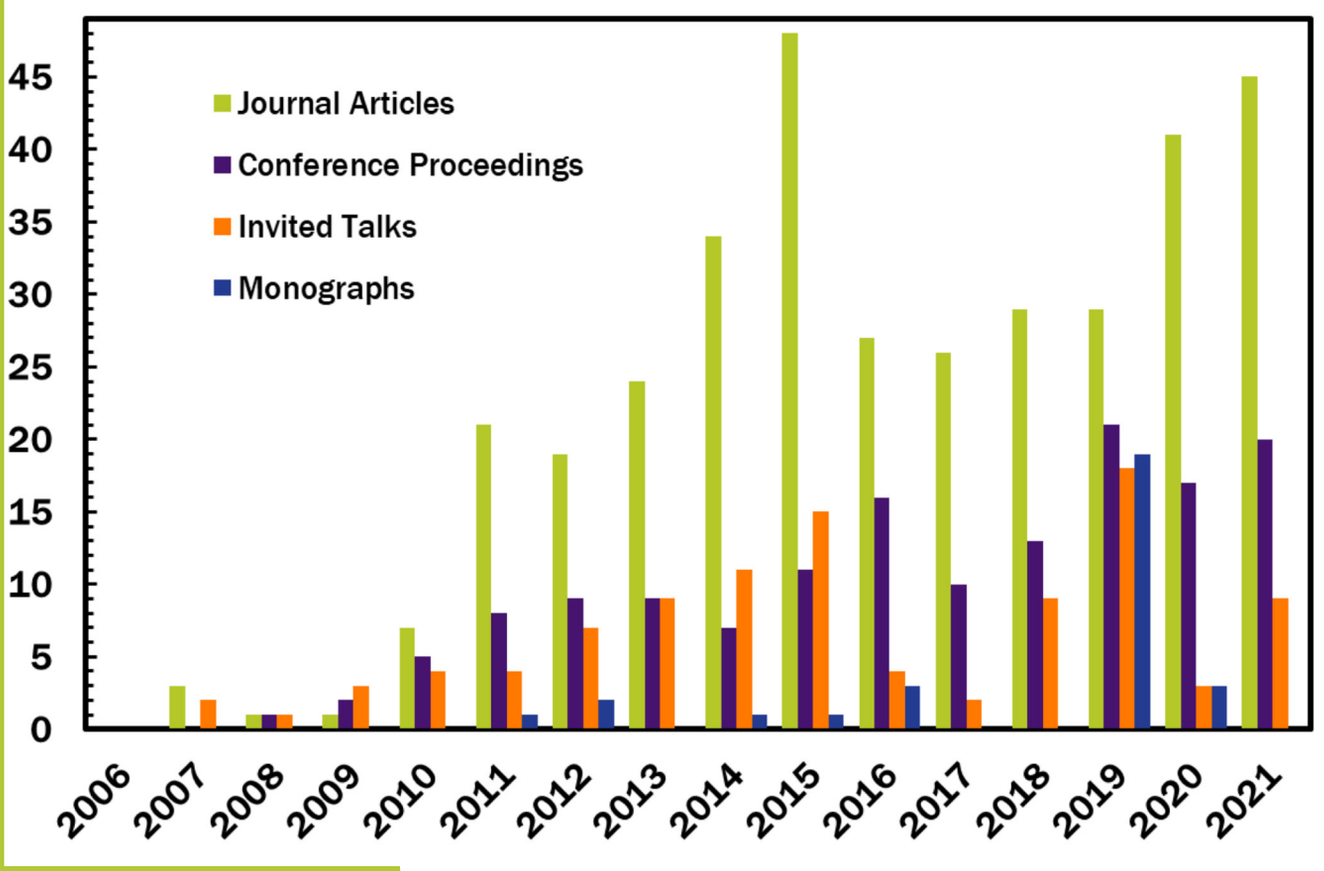

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