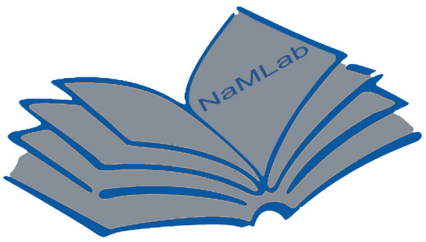
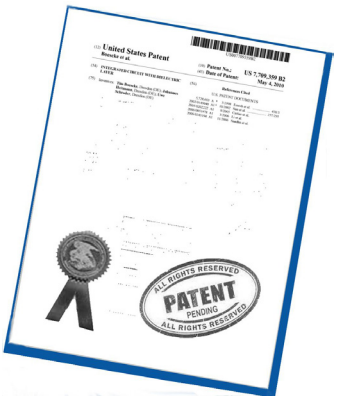

namlab
a tu dresden company
Two-Year Report
2018.2019

Highlights 2018/2019

Employees	PhD Students
42	14

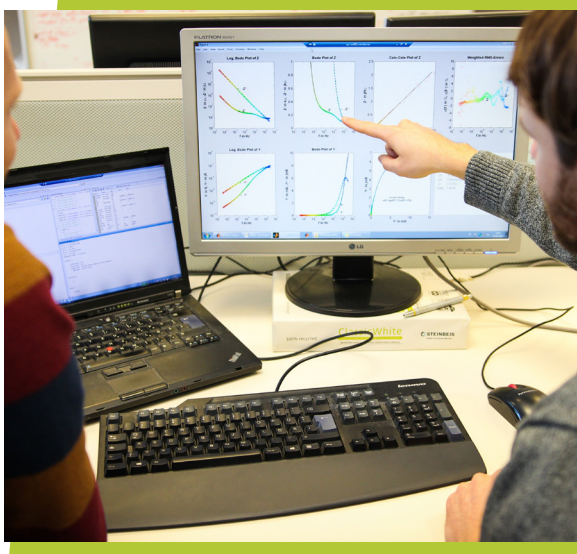


Publications	Citations
79	>4600



Patent applications/ Patents	Research Projects
11/6	21

Content



Prof. Dr.-Ing. Thomas Mikolajick

Preface

NaMLab was founded in 2006 as a public private partnership between Qimonda AG and TU Dresden. In the first year, NaMLab started as a research organization with 10 employees focused on material research for future memory devices. The company steadily expanded and today, NaMLab serves a growing list of world-wide partners. NaMLab's research is contributing to the main challenges for our future society with respect to climate change, digitalization and mobility by placing sustainable, secure and intelligent electronic solutions into the core focus. With respect to the technical areas those solutions can be divided into three main activities:

- Dielectrics for Semiconductor Devices,
- Reconfigurable Devices and
- Energy Efficiency Devices

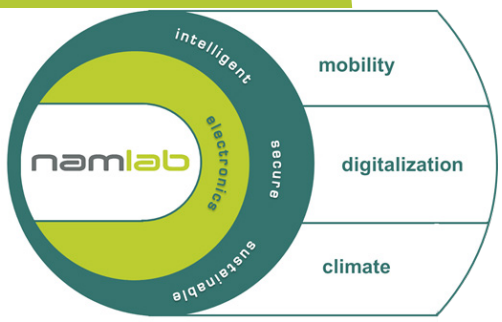
This fifth bi-annual report covers the NaMLab activities in the two year period 2018 and 2019. In that time frame, NaMLab further extended its role as a leading scientific research organization bridging basic research to application and industry. The level of international attention both for the scientific and the industrial environment has further increased.

NaMLab's research in the field of dielectrics is focused on flourite-structure ferroelectric materials, such as hafnium oxide, and their application in capacitors. The understanding of the main factors that control ferroelectricity in hafnium oxide, as well as the understanding of the degradation mechanism of such ferroelectric materials was further enhanced. The significance of the oxygen vacancy concentration for the stabilization of the ferroelectric phase was observed and unavoidable depolarization fields have been identified to have a major contribution to the polarization-voltage characteristics and the field cycling stability. Beyond, the research on dielectrics is strongly linked to the device oriented topics.

All three reconfigurable device concepts explored at NaMLab are currently under consideration for applications in both intelligent self-learning electronics as well as electronics with a higher inherent security.

In reconfigurable nanowire devices, the polarity of a field effect device can be controlled by applying a gate voltage to a dedicated programming gate. In the reporting period, the efforts to develop the concept up to the system level together with partners from TU Dresden have been further extended. An important ingredient on the technology side was the development of a top-down fabrication route that enables faster realization of more complex devices and circuits. A first ferroelectric Schottky barrier field effect transistor has been realized which further extends the reconfigurability of the device to the non-volatile regime.

The second topic in reconfigurable devices is field effect transistors based on ferroelectric hafnium oxide. Together with partners from Fraunhofer IPMS-CNT and GLOBALFOUNDRIES, NaMLab has pushed this concept since 2009. In the reporting period, NaMLab worked together with GLOBALFOUNDRIES and the NaMLab



The research activities of NaMLab are connected to the main societal challenges: mobility, digitalization and climate change by focusing on intelligent, secure and sustainable electronic devices.

Dielectric Materials

Capacitor Dielectrics
Flurite Structure Ferroelecrics

Reconfigurable Devices

Reconfigurable Nanowire Devices
Ferroelectric Devices
Resistive Switching Devices

Energy Efficiency Devices

GaN Devices
Dielectrics for Solar Cells
Anodes for Li-Ion Batteries

Overview of research activities at NaMLab

Spin-Off FMC on the further development of the embedded FeFET technology at GLOBALFOUNDRIES. Moreover, the focus shifted towards exploration of useful applications of ferroelectric hafnium oxide beyond semiconductor memories like negative capacitance field effect, neuromorphic computing and memory-in logic devices. The realization of both synapse and neuron circuits using FeFET devices were achieved. With respect to negative capacitance, NaMLab succeeded in the first measurement of the S-curve of a ferroelectric using a pulsed measurement technique.

The third major reconfigurable device concept explored is resistive switching. Here, new aspects of the threshold switching in niobium oxide have been explored that enable circuit demonstrators for new computing paradigms.

The field of energy efficiency devices has three key topics, namely solar cells, batteries and GaN materials and devices. All three research activities aim on providing sustainable electronic solutions. The focus of the field of solar cells was the development of conducting passivation layers building upon NaMLab's expertise in dielectric materials. Results showing the feasibility of the different components: conductivity and surface passivation have been successfully demonstrated. Based on the know-how in bottom-up nanowire fabrication, anodes for lithium-ion batteries were processed. In this reporting period a method to characterize the stability of silicon anodes using in-situ Raman spectroscopy was developed, which will be extended in the future.

In the field of gallium nitride materials and devices at the outpost in Freiberg, we were able to reproducibly fabricate crack-free doped HVPE GaN crystals that are suitable for wafering. At the same time, in the MBE activities high quality films that reflect the low dislocation density of the underlying layers can be achieved and heterostructures with an inherently absent 2DEG were reported for the first time. In the field of GaN devices, development the pseudo-vertical device was further optimized and a technique to extract the p-doping concentration in the bulk of the device using the body bias effect was established.

In summary, in the reporting period NaMLab could further strengthen its position in the core topics, contributing to the grand challenges of our modern society and therefore increased its reputation in both the scientific and industrial semiconductor communities. This is documented in the increasing number of partnerships with local and international industrial and research partners. Another impressive increase of citations of NaMLab's scientific publications as well as a large number of invitations to leading scientific conferences like IEEE-IEDM, VLSI, MRS etc. document the high international visibility NaMLab has now achieved. The NaMLab team will built on the strong results accomplished in this reporting period and further extend its efforts to continuously contribute to shape the exciting and challenging world of micro- and nanoelectronics.

Prof. Dr.-Ing. Thomas Mikolajick

NaMLab Team

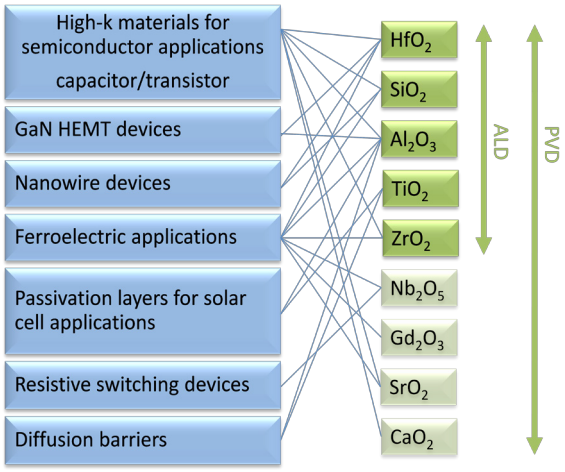
Dielectric Materials

Process control under an optical microscope.

Overview Dielectrics

Materials with high dielectric constant (high-k materials) play an increasingly important role in nanoelectronic devices. For example, in conventional semiconductors charge is stored in capacitors with a dielectric insulation layer. In order to maintain the storage capacity of capacitors, new dielectric materials with higher dielectric constants have to be introduced for devices with smaller area. Similar dielectric materials are needed for the next generation of high performance transistor devices as well as processors and logic products. A variety of research projects in the nano-scale regime are ongoing in order to gain an understanding of the influence of material properties with respect to leakage mechanisms, performance, speed and reliability.

As depicted in the schematic below, a set of five main material systems (Al_2O_3, HfO_2, TiO_2, ZrO_2, and SiO_2) is used for different dielectric applications. Accordingly, a detailed understanding of the structural and electrical properties gained on a device application can be used as a fundamental basic knowledge for future new devices. The impact of process properties on the device performance can be correlated. Especially, the optimization of charges and traps, dielectric constants, material properties like density, dielectric, piezoelectric, ferroelectric, and optical properties are important for the various device applications.



NaMLab also screens and characterizes further candidate materials like e.g. Nb_2O_5, SrO_2, and $CaTiO_3$ for novel device applications. Additional new dielectrics will follow. Materials are deposited by molecular beam deposition (MBD), atomic layer deposition (ALD), chemical vapor deposition (CVD), and physical vapor deposition (PVD) as shown in above drawing, Research at NaMLab covers a wide range of applications from dielectrics for nanowire transistors (Fig. 1), GaN HEMT devices (Fig. 2), capacitors to structures (Fig. 3).

Contact: Dr. Uwe Schroeder

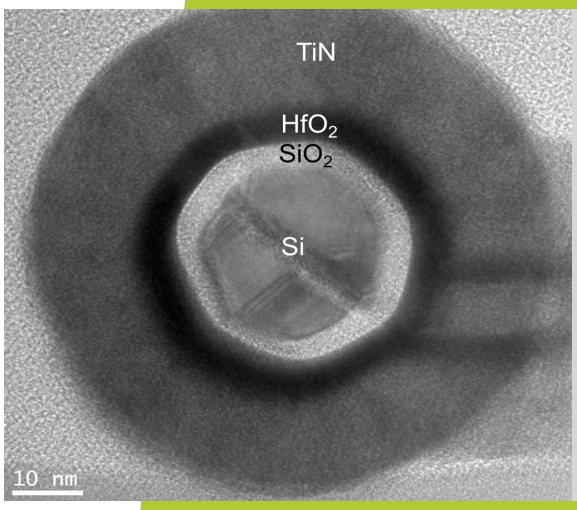


Fig. 1: ALD based dielectric materials as gate dielectric in nanowire and ferroelectric field effect transistors.

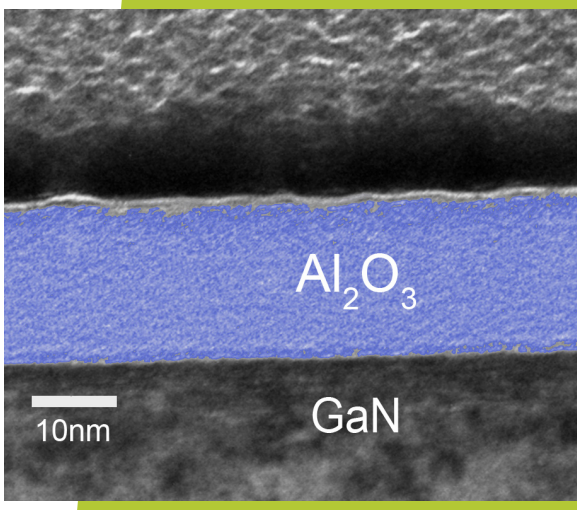


Fig. 2: Deposition of ALD Al_2O_3 dielectrics within a GaN HEMT device.

Fig. 3: Deposition of ALD $HfZrO_2$ dielectric in a capacitor structure.

Hafnium Oxide Based Ferroelectric Materials

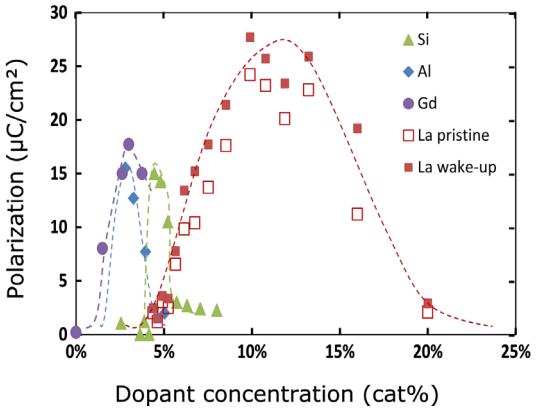


Fig. 1: Remanent polarization values for ~10 nm thick Si, Al, Gd, and La doped HfO_2 films with different dopant content.

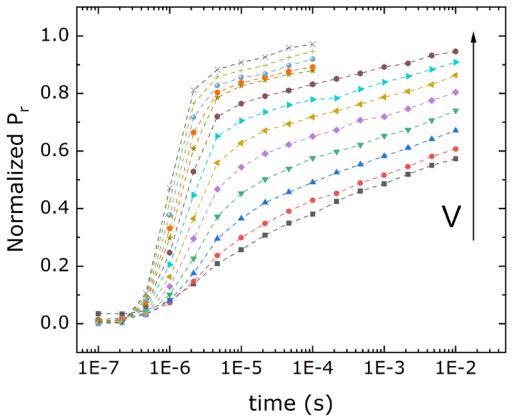


Fig. 2: Remanent polarization for different pulse times and voltages for a 10 nm thick HfZrO thin film capacitor showing the voltage-time trade-off to achieve domain switching.

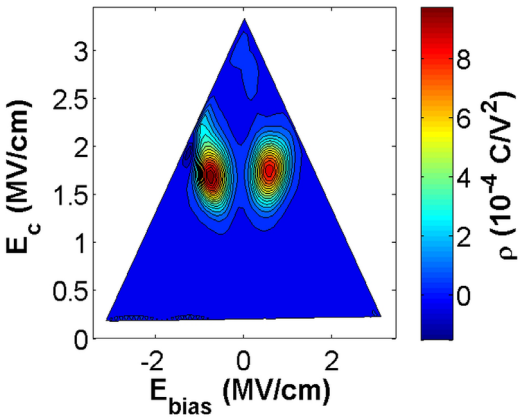


Fig. 3: First-order reversal curve measurement results of ~10 nm thick La doped HfO_2 films in capacitors. Internal bias field defined as the difference in E_{bias} of the maxima.

During the last two years the main focus of development of ferroelectric HfO_2 based materials is the detailed understanding of the ferroelectric properties in thin doped HfO_2 layers. A variety of dopant materials (Si, Al, Ge, Y, Gd, La and Sr) were studied in addition to a mixed $Hf_{1-x}Zr_xO_2$. A different ionic radius, smaller or larger than Hf and different valency can impact the phase formation (Figure 1). Deposition techniques included atomic layer deposition and physical vapor deposition. The ferroelectric orthorhombic $Pca2_1$ phase of HfO_2 is formed when the material is crystallized with a certain dopant or oxygen concentration at the phase boundary between the monoclinic and the tetragonal/cubic phase and is enhanced through mechanical confinement. Scanning transmission electron microscopy and electron diffraction methods confirmed the structure. Continuous research is ongoing aimed to understand the root cause of this previously unknown phase. In particular, the effect of interplay between the influence of different dopants and the amount of oxygen vacancies or interstitials present in the layer on phase formation is under investigation. A detailed analysis of Lanthanum doping confirmed the interaction between both. In fact, it was shown that two three-valent Lanthanum dopant atoms within a HfO_2 based layer introduced one oxygen vacancy. Surface and interface energy of these grains together with residual stress generated during growth and crystallization anneal can be additional critical parameters. Ab initio simulations by partners at the Munich UAS and University of Connecticut confirmed the influence of the above mentioned factors on the phase stability of ferroelectric HfO_2. A qualitative model describing the influence of these basic parameters on the crystal structure of HfO_2 was proposed.

The polarization hysteresis for all dopants showed a maximum remanent polarization value between 15-40 µC/cm², depending on the dopant material. The highest values were obtained for Lanthanum doped HfO_2 with TiN electrodes. Piezo-response force microscopy (Oak Ridge Nat. Laboratory/Univ. Nebraska) in conjunction with transmission electron microscopy (North Carolina State University) measurements revealed domains within single grains with a diameter of ~20-30 nm for 10 nm thick films. The polycrystalline structure of the films caused a varying polarization orientation within the layer. The size distribution of the grains follows a Poisson distribution resulting in a grain size dependent coercive field and Curie temperature.

Future studies will focus on the structural basis of the ferroelectric properties and their impact on the ferroelectric switching behavior and how device cycling performance can be improved.

Cooperation: Fraunhofer IPMS-CNT, Dresden (Germany), RWTH Aachen (Germany), UAS Munich (Germany), GLOBALFOUNDRIES Dresden (Germany), IMEC (Belgium), Oak Ridge National Labs (USA), Dalin University (China), North Carolina State University Raleigh (USA), Tokyo Institute of Technology (Japan)

Publications: J4-7, J14, J18-21, J23-25; J27, J30, J42, J47, J48, J52, J53, J55, M3, M10-14, I4, I5, I17, I25, I28, T3

Contact: Dr. Uwe Schroeder

Hafnium Oxide Based Piezo- And Pyroelectric Materials

The main focus of the work is on a detailed understanding of the pyroelectric properties (PE) in thin doped HfO_2 layers. Pyroelectric properties were characterized for various doped HfO_2 and mixed $Hf_xZr_{1-x}O_2$ films.

The ferroelectric and pyroelectric properties of 10 nm thick Si-doped HfO_2 capacitors in a Si-doping range of 1.6 - 3.8 at.% were investigated. The pyroelectric coefficient and figures of merit were used to assess Si-doped HfO_2 for infrared sensing and energy harvesting applications. The properties of Si-doped HfO_2 were observed to be paraelectric from 0 - 1.6 at.% Si, ferroelectric between 1.6 - 2.5 at.% Si, antiferroelectric at 2.5 - 3.5 at.% Si, and paraelectric again for higher Si-doping concentrations (Fig. 1). Such transformations in the electrical behavior of Si-doped HfO_2 with increasing doping were observed to arise from the stabilization of the nonpolar monoclinic to polar orthorhombic and then to the nonpolar tetragonal crystal phases with increasing Si-doping. A maximum in the pyroelectric coefficient, 46.2 $\mu C K^{-1} m^{-2}$, coincided with a maximum in the remanent polarization at 2.0 at.% Si. The pyroelectric coefficients in all of the Si-doped HfO_2 films were stable over a 0 - 170 °C temperature range which is very promising for sensing applications using the pyroelectric effect.

A survey of the pyroelectric behavior was undertaken for a wide variety of dopants incorporated into HfO_2 including Al, Gd, Sr, and La as well as the $Hf_{0.5}Zr_{0.5}O_2$ composition. $Hf_{0.5}Zr_{0.5}O_2$ exhibited the largest remanent polarization and the largest pyroelectric coefficient of 70 $\mu C K^{-1} m^{-2}$. Through the Landau-Devonshire Gibbs energy equation for a ferroelectric material, a relationship between the dielectric, ferroelectric, and pyroelectric properties was established by the Curie constant (Fig. 2). It was discovered that the Curie constant could predict the relationship between the remanent polarization, dielectric constant, and the pyroelectric coefficient independent of dopant type and doping concentration (Fig. 3). Pyroelectric performance can thus be predicted by the dielectric constant, remanent polarization, and Curie constant which is convenient for circuit designers and device integration. High aspect ratio and CMOS-compatible fabrication processes give HfO_2-based pyroelectric devices an advantage over other high-performance ferroelectric materials.

Upcoming studies will investigate the pyroelectric effect with new structures and operating conditions for sensing and energy harvesting applications.

Cooperation: RWTH Aachen (Germany), Hochschule München (Germany), Oak Ridge National Labs (USA), TU Bergakademie Freiberg (Germany)

Publications: J13, M1, M9

Contact: Dr. Uwe Schroeder

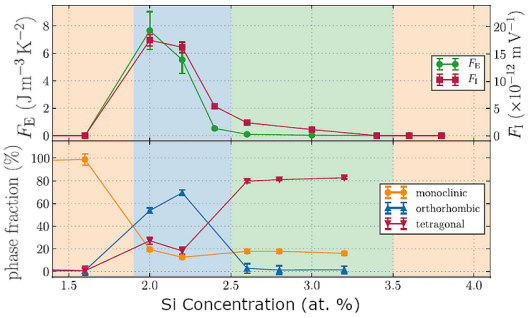


Fig. 1: Ferroelectric and pyroelectric properties with Si-doping.

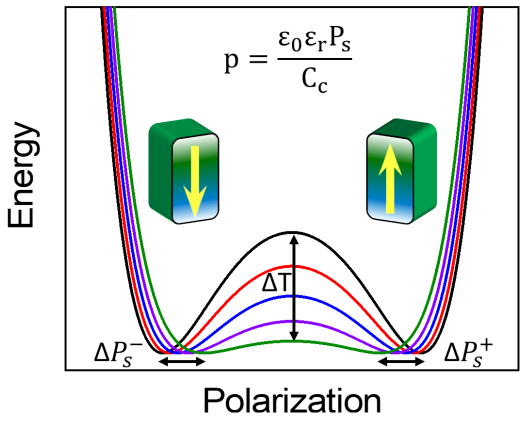


Fig. 2: Landau-Devonshire Gibbs energy diagram showing changes to the spontaneous ferroelectric polarization with temperature.

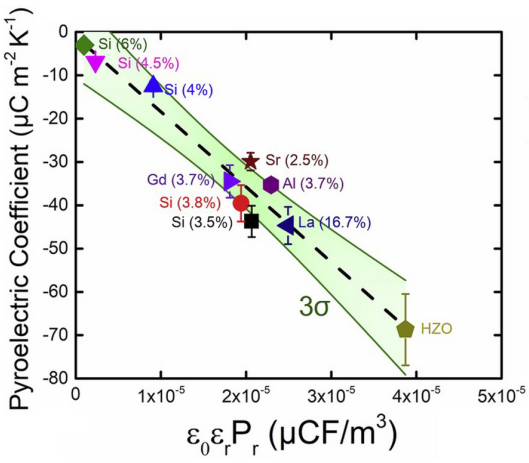
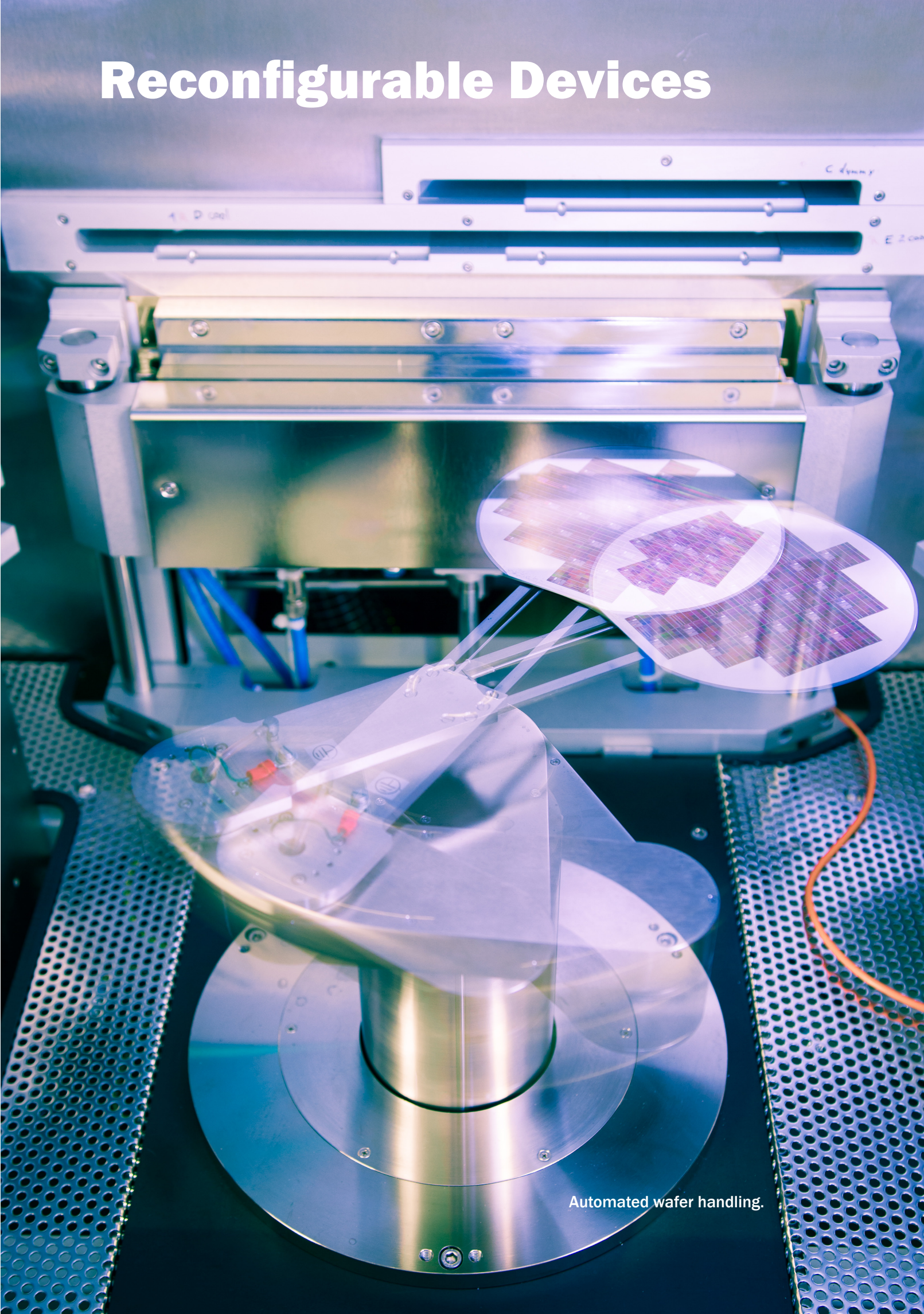


Fig. 3: Pyroelectric coefficient plotted against $\varepsilon_0 \varepsilon_r P_r$ for $Hf_{0.5}Zr_{0.5}O_2$, Si-, Al-, Gd-, Sr-, and La-doped HfO_2. The inverse slope of the line yields a Curie constant independent of dopant type.

Reconfigurable Devices



Automated wafer handling.

Capacitor Based Ferroelectric Memory

During the last two years the main focus was on the transfer of the metal-ferroelectric-metal capacitor stack with a capacitor diameter of about 100 µm to memory arrays with 100-1000 times smaller feature size. Concurrently, the optimization of the film and film stack properties to improve the reliability of the ferroelectric capacitor according to industry specifications was addressed. The goal is to develop a back-end-of-line (BEOL) compatible capacitor structure with a maximum thermal budget below 500 °C. The ferroelectric material of choice is an atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$. Development on the topic was carried out with industry partners like LETI, ST within a European project '3eFerro' and Sony.

The polarization hysteresis of a $Hf_{0.5}Zr_{0.5}O_2$ based capacitor showed a maximum remanent polarization value of about 25 µC/cm². In addition, the influence of Lanthanum doping in $Hf_{0.5}Zr_{0.5}O_2$ on the field cycling behavior was examined and a stable cycling behavior up to 1E10 cycles was achieved (Figure 1). Wake-up, internal bias fields, fatigue, imprint and retention effects in $Hf_{0.5}Zr_{0.5}O_2$ are generally dominated by charge trapping effects at defects mainly located in the $Hf_{0.5}Zr_{0.5}O_2$/electrode interface. Furthermore, depolarization effects can be caused by non-polar phases. Structural changes associated with field induced phases transitions are determined to be highly suppressed with less than 1 % changes in synchrotron-based diffraction measurements. The length of the oxidant pulse within the atomic layer deposition process plays a major role in the phase formation and the reliability properties of the capacitor structure (Figure 2). The duration of the ALD oxidant pulse strongly impacted the ferroelectric properties and an optimum process condition could be determined. Switching characteristics beneficial for non-volatile memory applications were then evaluated with optimum ferroelectric properties. Due to the resulting voltage-time trade-off to achieve > 90% domain switching after 10 ns, a voltage of about 2.5 V has to be applied to 10 nm thick films.

Both development partners introduced the $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric material into their memory arrays and reached a field cycling endurance > 10^{11} for sub 1 µm capacitor structures (Figure 3), good read voltage margin at 2.5 V operation voltage and confirmed an operating speed of about 10 ns for memory arrays of 16 or 64 kbit.

Future studies will focus on further understanding of the structural basis of the ferroelectric properties and their impact on the ferroelectric switching behavior, with the goal of improving cycling performance for introduction into larger memory arrays.

Cooperation: CEA Saclay / CEA-LETI (France), ST Microelectronics (France), National Institute of Materials Physics (Romania), EPFL (Switzerland), Ecole Centrale De Lyon (France), NCSR „DEMOKRITOS" (Greece), Forschungszentrum Jülich (Germany), Sony (Japan)

Publications: J16, C7, C21, C23, C24, C27, C33, M5, M16, M17, M18, I1 ,I2 ,I3, I6, I11, I12, I13, I14, I22, I23, I24

Contact: Dr. Uwe Schroeder

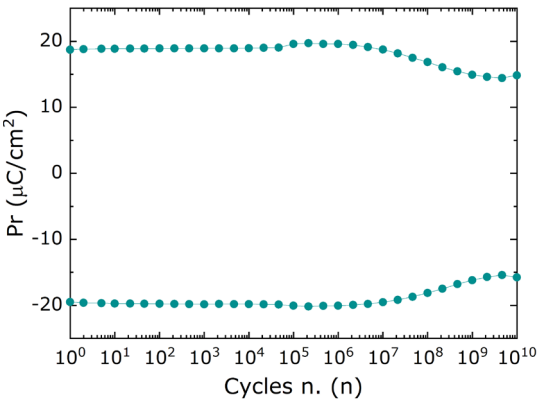


Fig. 1: Remanent polarization values for ~10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ based capacitor during field cycling.

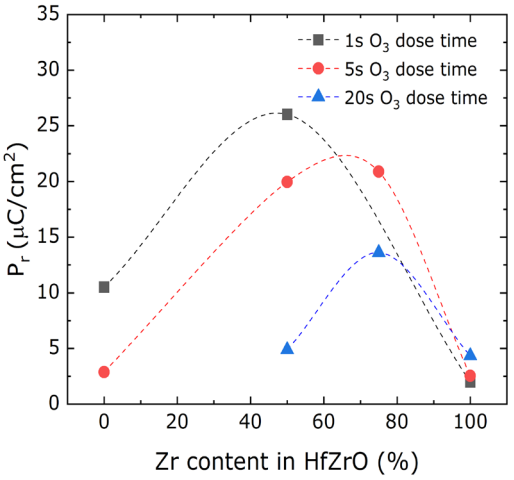


Fig. 2: Remanent polarization for $Hf_xZr_{1-x}O_2$ films with different oxidant dose times in capacitor structures with TiN electrodes.

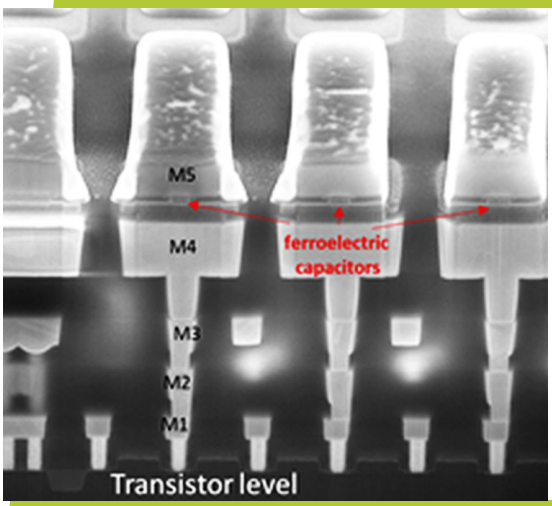


Fig. 3: SEM cross section of a 10 nm thick HfZrO films within a 16kbit capacitor-based memory array as fabricated within the 3eFerro EU project with partners LETI/ST (IEDM 2019).

FeFET Based Ferroelectric Memory

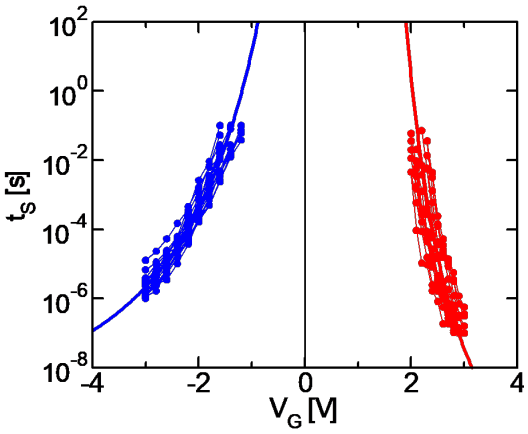


Fig. 1: Measured voltage-switching time trade-off of FeFET devices based on 28 nm technology. The measurement technique allows for the fast screening of switching kinetics and retention time.

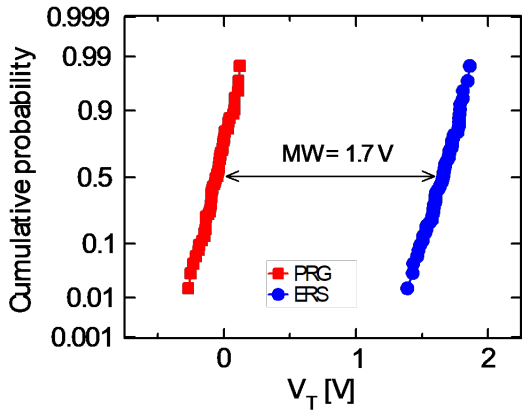


Fig. 2: Cumulative probability plot of low-VT and high-VT state of 63 FeFET devices measured in a passive memory array. The 9 nm thick ferroelectric layer exhibits a mean memory window of 1.7 V.

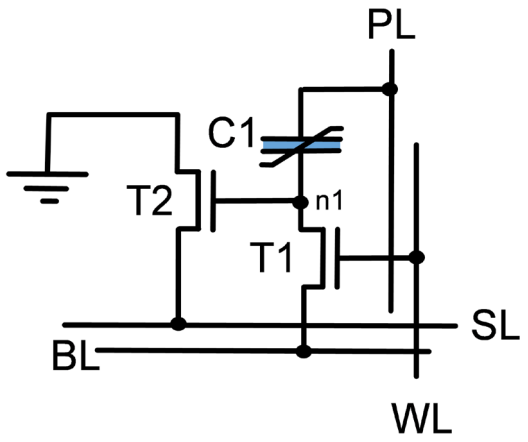


Fig. 3: A 2T1C ferroelectric memory cell for small scaled planar ferroelectric capacitors and ferroelectric tunneling junctions (FTJ). In this concept T1 is the access transistor while T2 provides a cell-internal signal gain.

HfO_2-based ferroelectric memories are long-term contenders for ultra-fast, low-power and non-volatile memory technologies. The electric polarization reversal in ferroelectric thin films is adopted in different memory devices. While the write operation is always conducted by applying an electric field in either polarity to the ferroelectric film, the read operation distinguishes three main concepts. In the FeRAM mode, the displacement current of a ferroelectric capacitor (FeCAP) is directly measured during polarization reversal, leading to a destructive read operation. In contrast, in the ferroelectric tunneling junction (FTJ) the polarization state dependent leakage current is measured and is indicative for the stored data. Finally, in ferroelectric field-effect transistors (FeFET) the information is stored as a polarization state of the gate dielectric and can be read non-destructively as a shift of the threshold voltage of the transistor.

In collaboration with GlobalFoundries and Fraunhofer IPMS FeFET devices were successfully implemented in a 28 nm gate-first super low power (28SLP) CMOS technology platform using only two additional structural masks. In our work we concentrate on the electrical characterization and modeling of the FeFET. The distinct electrical characteristics of these novel devices are analyzed in detail. Target is the comprehensive understanding of the interplay between different physical mechanisms that influence important memory characteristics such as cycling endurance or data retention as well as switching voltage and times. Fig. 1 reports the measured trade-off between the switching voltage and switching time for the program and erase operation of fully CMOS integrated FeFET devices. From this data it is possible to determine the optimum operation conditions and/or the retention time by extrapolation to 0 V gate voltage.

Fig. 2 depicts the superior memory window of up to 1.7 V that was measured in a passive array of 63 FeFET devices featuring a 9 nm thick ferroelectric film. The thickness of the ferroelectric has an impact on the memory window but also on the internal electric fields that are decisive for the data retention. With our results we aim at further optimizing the FeFET technology and to support our start-up company FMC (Ferroelectric Memory Company, www.ferroelectric-memory.com) targeting at the commercialization of the FeFET-based memory, which was developed in Saxony during the recent years. Besides device characterization and modeling we further engage in the development of memory cells and operation schemes that match the specific needs of the ferroelectric devices. Fig. 3 shows the schematic circuit diagram of our recently proposed 2 transistor 1 capacitor ferroelectric memory cell for the adoption of small scaled FeCAPs or FTJs.

Cooperation: GLOBALFOUNDRIES (Germany/USA), Fraunhofer IPMS-CNT (Germany), FMC (Germany)

Publications: J16, J44, J45, C7, C9, C11, C13, C23, C24, C27, C35, M6, M7, I1, I3, I6, I9, I13, I14, I20, I23, I24, I26

Contact: Dr. Stefan Slesazeck

Ferroelectrics For Beyond Von Neumann Computing

The increasing amount of data being processed in today's electronic devices for classification tasks in image and audio recognition, autonomous driving, smart sensors signal processing or machine learning, requires a transition from the conventional compute centric paradigm to a more data centric paradigm. In the classical von Neumann architecture, the data is transferred between computing and memory units via a bus system with limited bandwidth, giving rise to the well-known von Neumann bottleneck. In order to bridge the existing gap between memory and logic units, the concept of physical separation between computing and memory unit has to be repealed. FeFET devices co-integrated into CMOS can be adopted as localized storage element in digital logic circuits. One example is image processing, where e.g. images are fed as a serial data stream through a digital filter. Coefficients of the filter kernel are stored as digital values directly inside the logic circuit, as is depicted in Fig. 1. In this example, three FeFET devices are used as local digital memory elements in a dynamic full-adder circuit. While the digital computation has the benefit of a large signal-to-noise ratio, in analog computing circuits the data is represented by multiple intermediate states of a physical parameter such as threshold voltage of transistors or resistance of ferroelectric tunneling junctions (FTJ) and corresponding readout currents. These concepts benefit from the increase of information density per memory device, thus increasing the computation performance while lowering the power consumption per operation. Fig. 2 depicts an example by a logic-in-memory (LiM) operation. Multiple ferroelectric tunneling junctions (FTJ) that memorize digital data as different polarization states are read out in parallel. By evaluating the resulting sum current and comparing it to a threshold value I_{th}, different logic operations are realized. Brain inspired and neuromorphic computing emulates the vast parallelism of the biological archetype to boost the system performance. An extremely low power consumption is attained by adopting the concepts of synergized memory and computing functionality within one single device, an increase of information density by utilizing analogue switching mechanisms in densely connected convolutional neural networks, and the adoption of time dependent information processing where the temporal correlation between the signals contains additional information. The team investigates the adoption of FeFETs to realize artificial neuron circuits by making use of the accumulative ferroelectric switching effect. Fig. 3 depicts the measured integrate-and-fire functionality of a single FeFET device upon cumulative excitation with programming pulses of different amplitudes.

Cooperation: GLOBALFOUNDRIES (Germany/USA), École Centrale de Lyon (France), University Bielefeld (Germany)

Publications: J15, J17, J41, C1, C3, C6, C7, C8, C18, C22, C28, C30, C31, C32, M2, M8, I8, I16, I21, I23, I24, I27

Contact: Dr. Stefan Slesazeck

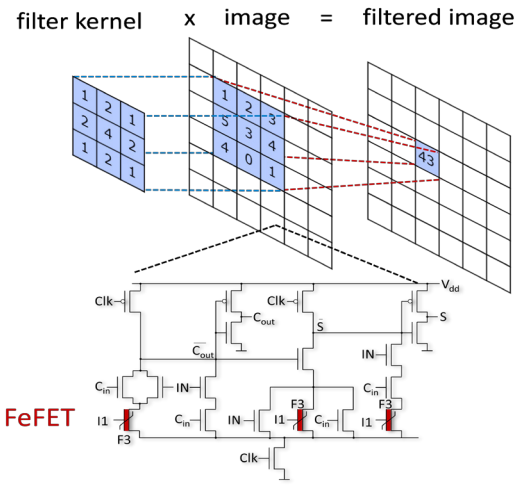


Fig. 1: Concept of a digital filter with filter coefficients stored locally within the logic circuit by the adoption of FeFET memory devices.

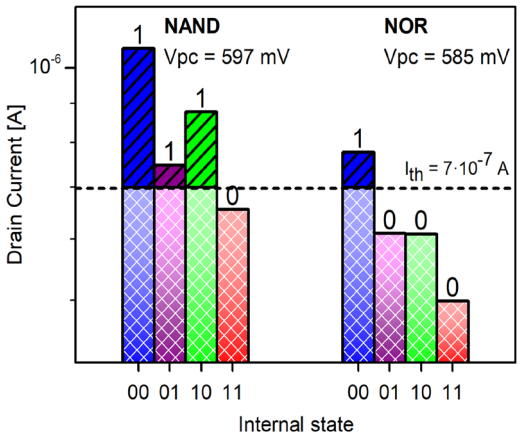


Fig. 2: Measured sum currents from FTJ-based LiM cells during readout operation. Different logic operation can be realized by comparing the sum currents to a fixed threshold value I_{th}.

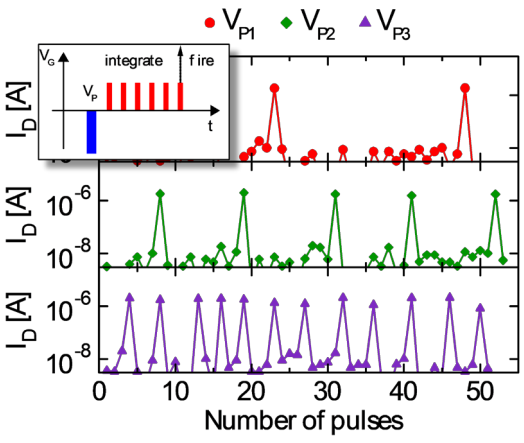


Fig. 3: The accumulative switching in FeFETs can be utilized to realize electrically tunable integrate-and-fire neurons for the adoption in spiking neural networks. Different excitation voltages lead to different spiking frequencies.

Negative Capacitance Devices

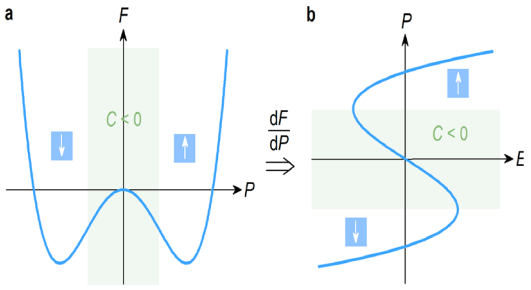


Fig. 1: a) Double-well energy landscape of a ferroelectric. b) S-shaped polarization-electric field curve showing negative capacitance.

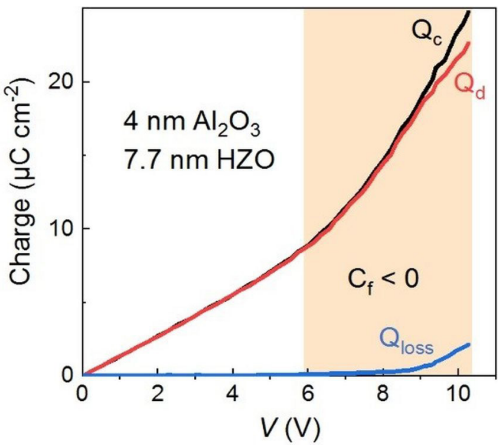


Fig. 2: Charge (-voltage) characteristics of a negative capacitance supercapacitor.

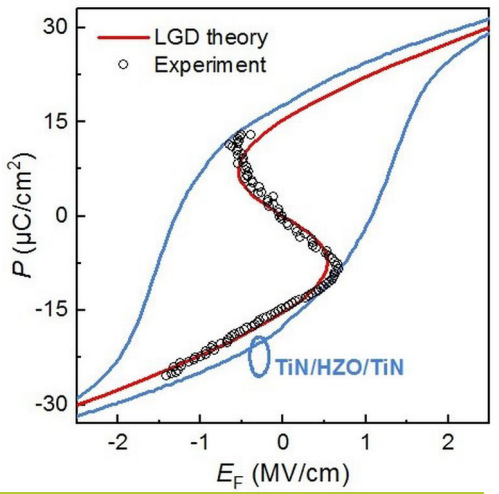


Fig. 3: First measurement of the S-shaped P(-E) curve in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$

Since the 1940's, phenomena in ferroelectric materials have been successfully modelled based on the Landau theory of phase transitions, which was first applied to ferroelectrics by Ginzburg and Devonshire. Phenomenological models based on this Landau–Ginzburg–Devonshire (LGD) approach have been an essential tool in understanding the basic physics of ferroelectricity. In LGD theory, a ferroelectric below its transition temperature is described by a double-well free energy landscape F as a function of the polarization P (Fig. 1a). The two degenerate energy minima define two stable spontaneous polarization states in the material, which can be reversed by the application of an electric field. By differentiating F with respect to P, one obtains the 'S'-shaped P(–E), where E is the electric field in the ferroelectric (Fig. 1b). This 'S'-shape of the P(-E) curve implies that in a certain region around P≈0 the ferroelectric possesses a negative differential capacitance (NC), because the capacitance C is proportional to the slope dP/dE, which is a direct consequence of the energy barrier in the double-well free energy landscape.

In theory, NC can be used to increase the capacitance of a dielectric layer by adding a ferroelectric layer and as such promises the realization of highly power efficient high-performance devices and supercapacitors (Fig. 2). NaMLab's research in this field focusses on the verification and physical understanding of the NC effects in ferroelectric HfO_2. Thereby, all the physical and electrical boundary conditions are considered, such as the influence of electrodes, additional layers in multi-layer stacks or the domain dynamics in the ferroelectric layer itself. The work performed at NaMLab includes the fabrication, physical and electrical characterization as well as modeling of ferroelectric capacitor-based devices.

The major goal of NaMLab's research is the development and optimization of novel device concepts and operation principles based on the NC effect. Due to the strong expertise in the field of ferroelectric HfO_2, NaMLab was able to directly measure the NC effect predicted by LGD theory for the first time in this material. This groundbreaking result was recently published in the prestigious journal Nature (Fig. 3), positioning NaMLab at the forefront of the international research on this topic. In a joint project with GLOBALFOUNDRIES negative capacitance transistors are being realized based on the already established FeFET integration flow. Future work will explore further applications of NC e.g. in energy storage supercapacitors.

Cooperation: GLOBALFOUNDRIES (Germany/USA)

Publications: J10, J11, J36, J37, C4, C5, C20, C29, M4, I15

Contact: Dr. Stefan Slesazeck

Reconfigurable FETs On A Top-Down SOI Platform

A promising concept to leverage computing power beyond conventional Moore's scaling is to extend the functional diversity of the basic electronic device, the transistor. NaMLab´s unique reconfigurable nanowire approach focuses on establishing a multifunctional electronics platform able to perform a higher number of functions with the same hardware complexity as conventional CMOS electronics. The reconfigurable nanowire field effect transistor (RFET) conceived at NaMLab and introduced already in 2008 is a four-terminal device that provides unipolar n- or p-type electrical characteristics at runtime as selected by an electric select signal (Fig. 1). Importantly, these devices are obtained without the need for doping and can by principle be fabricated with materials and processes established in volume silicon CMOS production facilities.

To enable the demonstration of more complex circuits and possible co-integration into modern CMOS flows the RFET technology was transferred from a bottom-up fabrication route to top-down process based on silicon on insulator (SOI) substrates. An omega shaped metal gate was used to increase the control over the nanowire channel. Thereby, stressor shells were successfully applied as enabler for symmetric drain-currents ensuring complementary operation of digital circuits. As an alternative method of barrier tuning, As dopant segregation after silicide contact formation has been studied. Different methods to control and reduce the variability in silicidation length of nanowires were established making the lab scale prototyping of simple demonstrator circuits possible. Appling those techniques, the RFET concept was extended to include a higher number of independent steering gates allocated along the channel (Fig. 2). The multi-independent-gate (MIG) approach efficiently bundles serial chains of FETs in a single device sparing interconnects and area for isolations, contacts and implantation wells. The MIG-RFET inherently provides a wired-AND function useful in many multi-input combinational circuits, such as majority gates or multiplexers.

In order to complement the work on horizontal RFETs, a feasibility study of RFETs based on vertically top-down nanowires was conducted by 3-D device simulations. Subdividing the RFET structure into two vertical pillars allows a lean technological realization as well as simple access to the electrodes (Fig. 3). We show that by the integration of additional vertical pillars and select gates, a higher device functionality and flexibility in interconnection are provided.

Cooperation: CfAED - Center of Advancing Electronics Dresden (Germany), DCN - Dresden Center for Nanoanalysis (Germany), Helmholtz Center Dresden Rossendorf (Germany)

Publications: J1, J39, C12

Contact: Dr. Jens Trommer

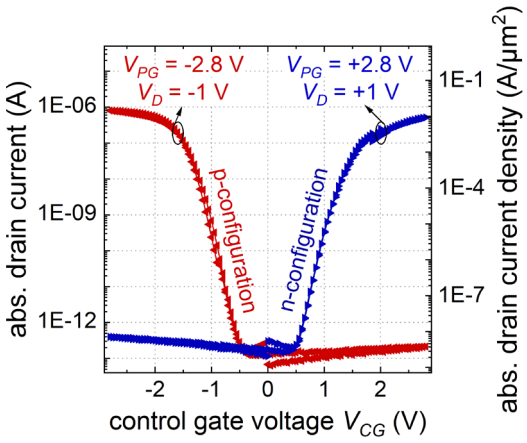


Fig. 1: Transfer characteristics of an RFET with selectable p-type (red) and n-type (blue) functionality built from a top-down SOI platform.

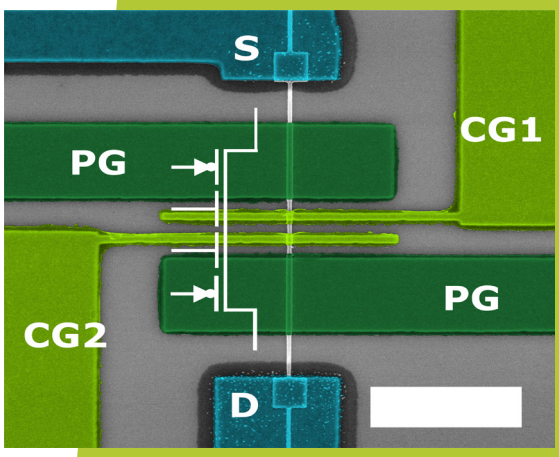


Fig. 2: Top-view SEM image of a nanowire MIG-RFET built from a top-down SOI platform. Two individual control gates (CG) and two externally connected program gates (PG), source (S) and drain (D) are labeled. Scale bar is 2 µm.

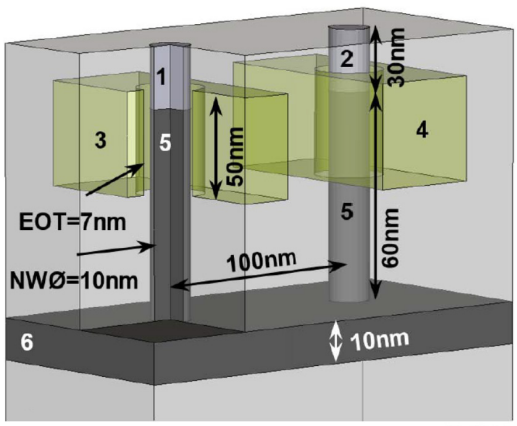


Fig. 3: Concept study of a vertical nanowire RFET integration on two pillars which are joined on an SOI body.

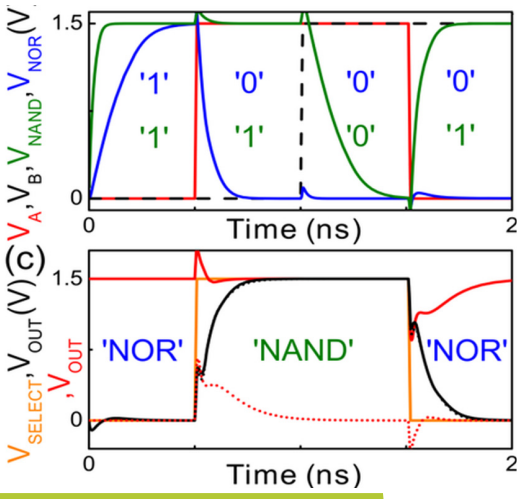


Fig. 1: Mixed-mode simulations: runtime-reconfigurable operation of a NAND/NOR circuit cell with 6 transistors. The cell always delivers full swing output.

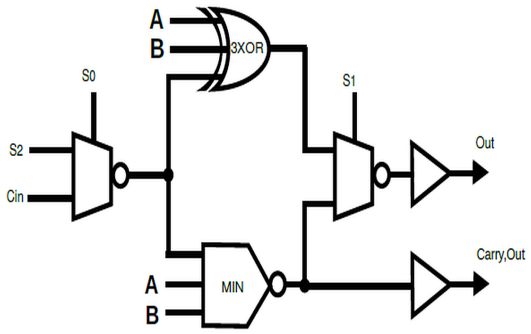


Fig. 2: Circuit schematic of a simple 1-bit ALU, exploiting runtime-reconfigurable logic gates.

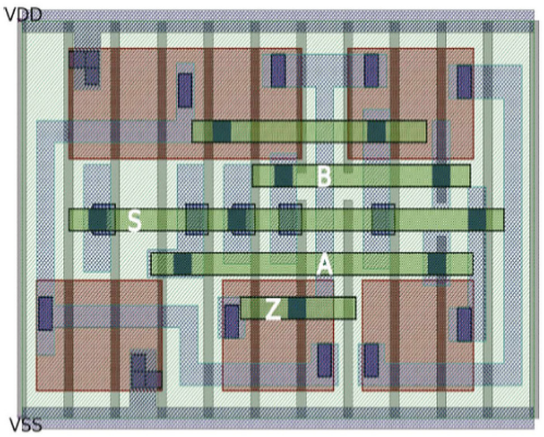


Fig. 3: Layout of a NAND/NOR cell compatible with 22 nm FDSOI design rules. The cell provides the same functionality as shown in Fig. 1.

Runtime-Reconfigurable Circuits

The multiple operation states of reconfigurable FETs open new opportunities for logic circuit design. Mainly, two features that were previously not accessible with conventional FETs are currently being studied. First, runtime-reconfigurable logic gates can be built, providing multiple functionalities as programmed on the fly by volatile select signals. Due to this reconfigurability, the overall value per building block is increased. One basic example is given by the compact cell, which can switch from NAND to NOR operation (Fig. 1). Distinctly, those cells always operate in a complementary manner, reaching a full swing output and exhibiting the same delay for both functions. The second feature is the integration of multiple gate electrodes along the nanowire channel, merging paths of series transistors within a single one, without increasing the internal resistance of the individual device. This feature can be exploited to build efficient XOR and Majority gates. Further, we recently showed the potential of such MIG/RFETs in dynamic logic gates as an elegant solution to reduce signal integrity risks such as the charge sharing effect.

Based on our RFET device results, we have shown a comprehensive library of reconfigurable logic gates and combinational circuits. Promising examples are adders and arithmetic logic units (ALU) that are important elements of modern CPUs. An example of simple ALU exploiting the reconfigurable nature of our devices is shown in Fig. 2. We have demonstrated that RFETs based circuits can achieve a smaller overall area than equivalent circuits in CMOS, albeit the individual devices are larger. In addition, critical delay paths can be significantly improved, leading to a reduction of the overall structural delay on the system level by approximately 50%, under the constraint, that an similar individual device performance can be achieved.

To enable advanced and complex circuit design with RFETs the setup of a fully automated synthesis route was necessary, especially since RFET circuit design is fundamentally different than CMOS design. In cooperation with the excellence cluster CfAED at TU Dresden, automated logic and physical synthesis tools were developed making it possible to design deliberate logic circuits and to deliver the required layouts compatible with design rules of a 22 nm FDSOI technology (Fig. 3). With this route it is possible to assess and to perform benchmarks of the associated delay, power consumption and area use per function.

Cooperation: cfaed - Center of Advancing Electronics Dresden (Germany)

Publications: J50, C10, C34

Contact: Dr. Jens Trommer

Germanium Nanowire RFETs For Performance Boosting

We have experimentally demonstrated the world-wide first transistor based on germanium that can be programmed between electron- (n) and hole- (p) conduction, Fig. 1. The reconfiguration is realized by changing the voltage applied to one of the gate electrodes. This option enables to realize circuits with lower transistor count compared to state-of-the-art CMOS technologies. Additionally, Transistors based on germanium can be operated at low supply voltages and reduced power consumption, due to the low band gap as compared to silicon.

The approach taken solves one of the limitations in using low-bandgap channel materials such as germanium and indium-arsenide. In conventional MOSFETs made from those materials the off state is strongly degraded by a high static current and associated power loss, also originating from their small band gaps. The off-currents can be drastically reduced by the blocking potential induced by the program gate.

We have verified by measurements and simulations, that supply voltage can be reduced by a factor of 2 and dynamic power consumption can be about 4 times lower compared to silicon based RFETs. In addition, on currents can be boosted by up to a factor of 10 without degradation of capacitances, see Fig. 2. This translates into a switching delay reduction of up to a factor of 10. For different device geometries performance and power consumption metrics were extracted and benchmarked with modern conventional devices, see Fig. 3. Scaled Ge RFETs are competitive compared to other modern low standby and operating power technologies. The performance boosting at the device level combined with the circuit capabilities of RFETs hold the promise of enabling new ground breaking circuit applications.

Within the reporting period, NaMLab and its partners evaluated optimal designs, layouts, and sizes for Ge based RFET using TCAD simulations. Results indicate a largely improved performance in conjunction with negligible increase in dynamic power consumption. Currently, SPICE-compatible Table models for circuit development with highly scaled Ge nanowire RFETs are under development. Target applications are hardware security, asynchrony computing and self-learning neuronal networks.

Cooperation: cfaed - Center of Advancing Electronics Dresden (Germany)

Publications: C2, M19

Contact: Dr. Jens Trommer

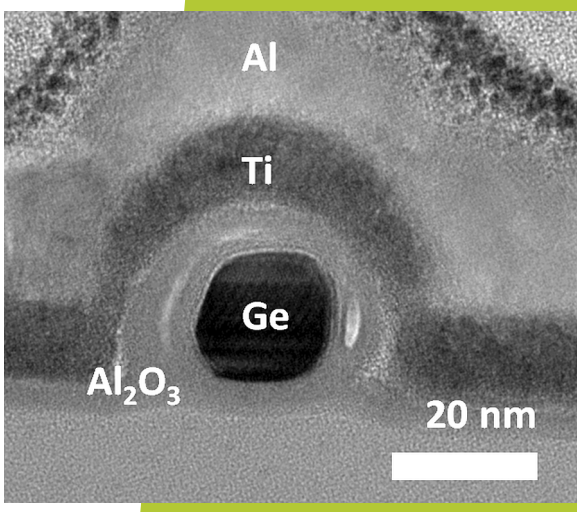


Fig. 1: Cross section image of germanium nanowire RFET with high-k/metal gate stack in omega shape.

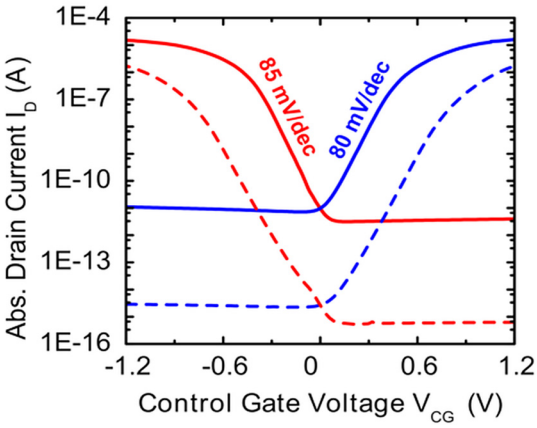


Fig. 2: Comparison of transfer characteristics of silicon (dotted) and germanium (solid) based RFETs as determined by TCAD simulations.

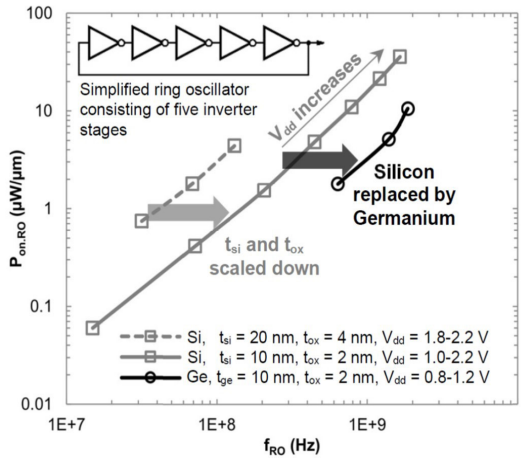


Fig. 3: Comparison of dynamic power vs. operation frequency of five-stage ring oscillators constructed of Si and Ge nanowire based RFETs.

Non-Volatile Programmable Nanowire FET Concepts

Classical RFETs employ a volatile electrical signal to dynamically program the functionality of the device, i.e. p- and n-conduction are steered only upon constant biasing of the program gates. We currently develop an option to store information within nanowire device for a longer time. Apart from classical data storage applications, this is of interest for hardware security, memory-in-logic and machine learning applications. For all those applications it is beneficial to store not only one, but multiple bits in a single cell. Currently, two approaches towards RFETs with embedded and non-volatile memory function are developed at NaMLab, a) the implementation of electron and hole trapping in silicon-oxide/-nitride based gate stacks and b) the integration of polarizable ferroelectric hafnia-zirconia based gate stacks.

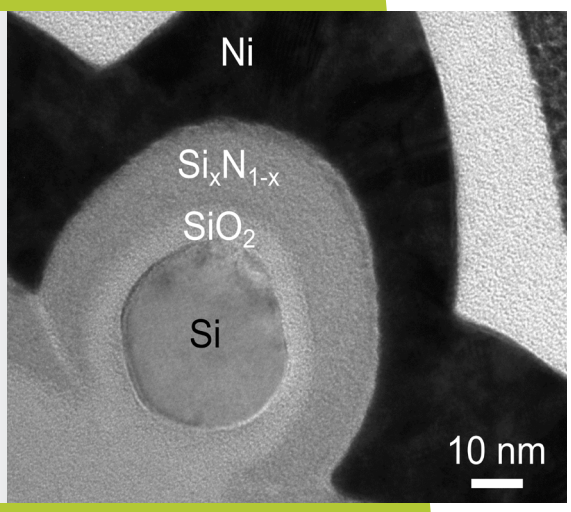


Fig. 1: Cross-sectional TEM of an omega shaped MNOS gate stack for the realization of a charge trapping based memory functionality in a reconfigurable field effect transistor.

As a first functional demonstrator a charge-trapping stack based on SiO_2, Si_XN_{1-x} and a Ni metal gate (SONM stack in Fig. 1) was incorporated in omega shape around the nanowire channel of a dual gated RFET. The device was programmed in four distinct operation modes by volatile programming the polarity gate to differentiate between p- and n-type behaviour, and non-volatile programming the control gate to attain the set vs. the reset state that is represented by the threshold voltage of the device (Fig. 2). The four distinct operation modes can be changed reversibly when programming / erasing the two gates by application of respective voltage pulses in either polarity.

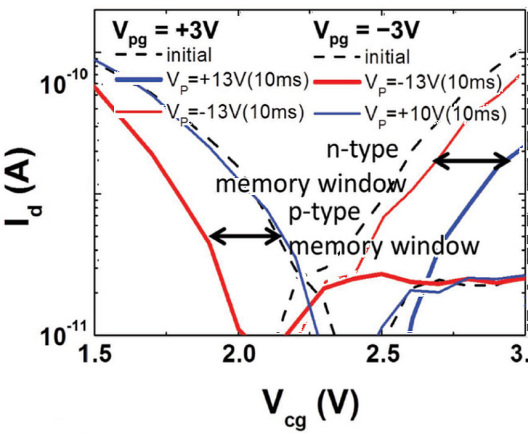


Fig. 2: Set and reset characteristics for a RFET with MNOS charge trapping gate. A non-volatile threshold voltage shift is achieved for both p-type and n-type mode.

In order to reduce the operation voltage and increase the stability of the non-volatile programed function currently the integration of a ferroelectric gate material is developed. The main challenge here, as compared to charge trapping layers, is to yield a stable crystallization of the individual grains with respect to the three-dimensional channel. Single gate Schottky FETs with Al-doped HfO_2 as well as $HfZrO_2$ ferroelectric materials were tested. Good results have been achieved on a trapezoidal nanowire etched from an SOI substrate (Fig. 3) demonstrating effective junction tuning between programmed (high V_{TH} and low I_{ON}) and erased (low V_{TH} and high I_{ON}) state. Our current work focuses on optimizing etching processes of HZO for dual gate implementation, the enlargement of the memory window and improvement of the endurance and retention properties.

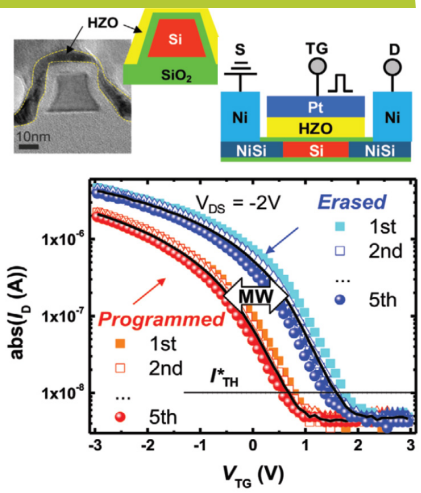


Fig. 3: A top-down fabricated nanowire Schottky FET with ferroelectric HfZrO (HZO) gate stack. Stable programmed and erased states are achieved.

Cooperation: CfAED - Center of Advancing Electronics Dresden (Germany), DCN - Dresden Center for Nanoanalysis (Germany)

Publications: J22, C11, C25

Contact: Dr. Jens Trommer

Resistive Switching Devices

The central aim of the research on Resistive Switching Devices is the development of materials and device structures, capable of changing their electrical resistance or capacitance by applying external voltages. The resistive memory device – the so called ReRAM – is one of the potential candidates for the realization of novel memories or storage class memory, since it is characterized by very fast access times, non-volatility, and low power consumption. A further interest for the adoption of these devices - which in the context of electronic circuit theory are also referred to as memristors - is the application of such reconfigurable devices in neuromorphic nano-circuits, exhibiting the united functionality of logic and memory in one device. NaMLab's activities cover the deposition and modification of dielectric thin films and electrode layers, the physical and electrical characterization as well as the modeling of the switching properties.

NaMLab's research focuses on niobium oxide (NbO_x) based resistive switching devices. By variation of the fabrication process, electrode materials and thin film composition a large variety of different switching characteristics could be obtained. One of these characteristics is a thermally induced Poole-Frenkel conduction-based threshold switching effect that manifests itself by a negative differential resistance (NDR) branch in the current-voltage characteristics. Fig. 1 shows how the voltage extension of the NDR region ΔV_{NDR} can be optimized by adjusting the thickness of the NbO_x bottom layer within the multi-layer device. Experimental results reveal the prediction from simulations that are based on aphysical model description of these devices. ΔV_{NDR} is an important parameter that defines the operation point when adopting these locally active devices e.g in oscillator circuits.

Fig. 2 shows a photograph of a circuit demonstration of two coupled locally active oscillators. The threshold switching devices were manufactured at NaMLab and were packaged by wire bonding so that they can be connected to complex circuits without suffering e.g. from parasitic cable capacitances that are unavoidable when probing the devices directly on silicon wafers.

A joint technology and design co-development is of utmost importance for advancing the technology readiness level of a novel device from the proof-of-concept (TRL 3) towards demonstration of the principle towards the component validation in a laboratory or even relevant environment (TRL4-5). In order to bridge the gap between the laboratory research and first industrial tests, NaMLab develops hybrid integration concepts where the novel devices are integrated into the back-end-of-line (BEOL) of standard CMOS chips (Fig. 3).

Cooperation: Helmholtz Center Dresden Rossendorf (Germany), TU-BAF (Germany), RWTH Aachen (Germany), University of Helsinki (Finland), TU Dresden (Germany), GLOBALFOUNDRIES (Germany), Fraunhofer IPMS (Germany)

Publications: J15, J33, J34, J56, J57, C26

Contact: Dr. Stefan Slesazeck

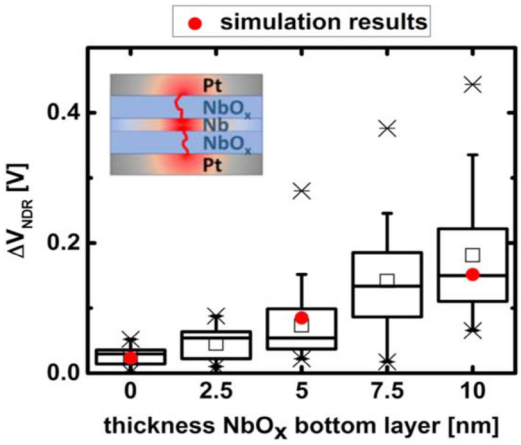


Fig. 1: Simulated and measured extension of the negative-differential resistance region ΔV_{NDR} in niobium oxide-based threshold switches.

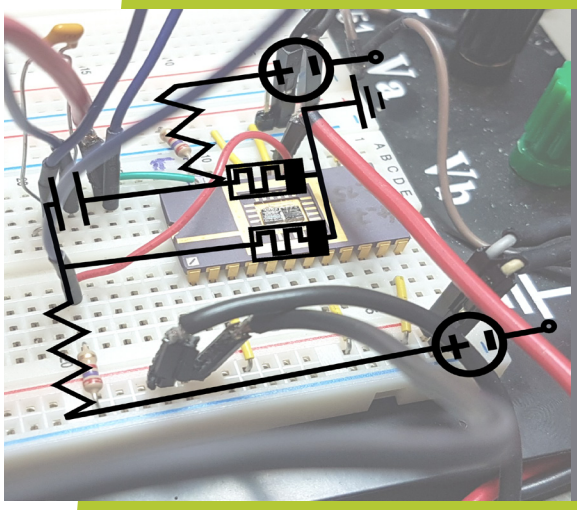


Fig. 2: Circuit realization of coupled oscillators based on locally active niobium oxide based threshold switches.

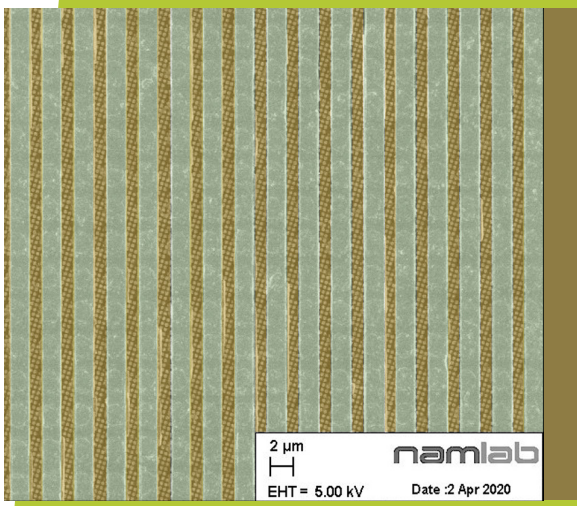


Fig. 3: Top-down SEM image of a 64kbit ReRAM test chip. The orange regions show the metal 5 layer of the underlying 28nm CMOS chip, while the green stripes are the top-electrodes manufactured at NaMLab.

Energy Efficiency Devices

Measurement of carrier lifetimes in solar cells.

Si-Nanowire Electrodes For Li Based Batteries

Lithium ion batteries (LIBs) have been a subject of an intense research since their first commercialization more than 25 years ago. The development of high capacity electrode materials is the most critical limiting factor to progress to the next generation batteries for electric vehicles. In the case of anode material, silicon has the highest theoretical capacity (3579 mAh/g), which is ten times more than the capacity of the state-of-the-art material graphite (370 mAh/g). However, silicon anodes experience dramatic volume change during lithiation and delithiation of more than 300 %, which leads to pulverization of anode material, unstable solid electrolyte interface formation and subsequent battery failure. In order to solve these problems, nanostructured anode materials (e.g. nanoparticles, porous nanoparticles, nanowires, double-walled nanotubes) have been extensively studied.

The NaMLab gGmbH is focusing on these challenges by developing new high capacity anode structures using Si nanowires as anode material (Fig. 1) and integrating those with the help from strong partners in research and industry into novel LIBs. The Si nanowires are subsequently coated with a highly conductive pyrolytic carbon coating (Fig. 2) established at NaMLab to improve the chemical and mechanical stability while ensuring a continuous electrical contact to the carbon current collector during long-term cycling. A stable operation of carbon coated Si nanowires in a LIB with a high capacity of 4 mAh/cm^2 at high charge/discharge rates for more than 600 cycles has been demonstrated. As the capacity per weight is the most important criteria for batteries targeting automotive applications, the binder-free high capacity Si nanowire anodes directly grown on a light-weight carbon based current collector give a unique opportunity for ongoing studies related to the integration in cell designs for batteries, which are relevant for application.

Furthermore, NaMLab is developing an in situ-Characterization of the solid electrolyte interface at the Si anode by employing Raman-Spectroscopy. This is a non-destructive way to determine the components of the anode, the electrolyte and their interface. It allows the monitoring of compositional and structural changes during the charging and discharging processes. Thus, the mechanisms of degradation can be investigated in real-time (Fig.3). The strong collaboration with our partners Fraunhofer IWS, IKTS, the Leibniz institute IFW and the TU Dresden within the framework of the projects “BaMoSa” and “KaSiLi” yielded full cells with Si nanowire anodes involving Li-Ion and Li-sulfur chemistry up to the pouch cell level.

Cooperation: Fraunhofer IWS, Dresden (Germany), Fraunhofer IKTS, Dresden (Germany), Fraunhofer IFAM, Dresden (Germany), Leibniz-Institute IFW, Dresden (Germany), Leibniz-Insitute IPF, Dresden (Germany), TU Dresden (IAC, IfWW, IOF), Dresden (Germany)

Publications: J40

Contact: Dr. Matthias Grube

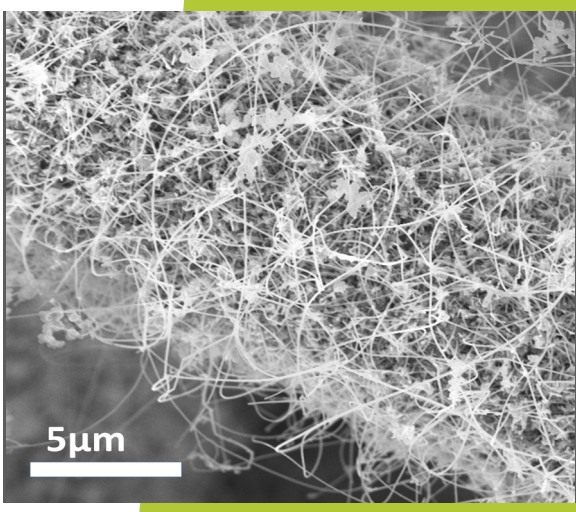


Fig. 1: Scanning electron microscopy (SEM) of a dense array of Si Nanowires grown by CVD on 3D carbon meshes.

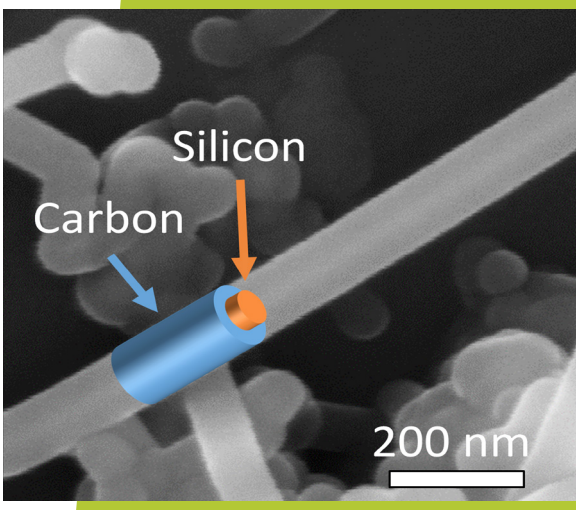


Fig. 2: SEM image of a single Si nanowire coated with an extremely uniform pyrolytic carbon layer.

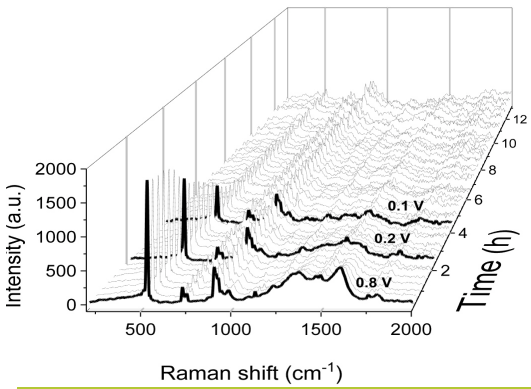


Fig. 3: In situ Raman-Analysis of a Si nanowire anode coated with pyrolytic carbon

Gallium Nitride Hydride Vapor Phase Epitaxy

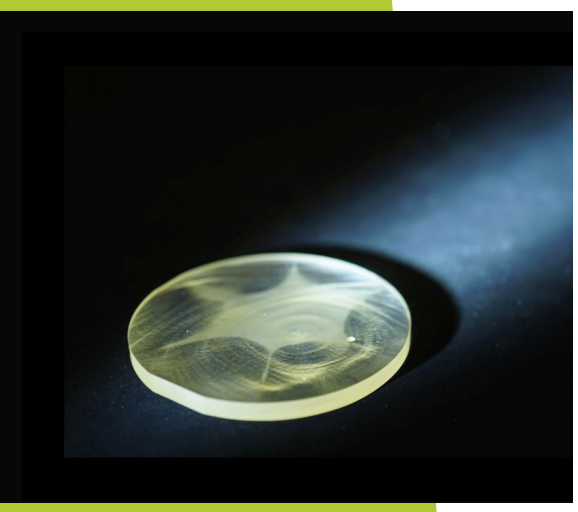


Fig. 1: Unintentionally doped (UID) 2“ round-ground GaN crystal grown on a template optimized for self-separation. It is about 5 mm thick with a smooth and specular surface.

Fig. 2: Ge-doped 2“ round-ground GaN crystal grown on a template optimized for self-separation. It is about 5 mm thick with a smooth and specular surface. The shading is coming from the separation.

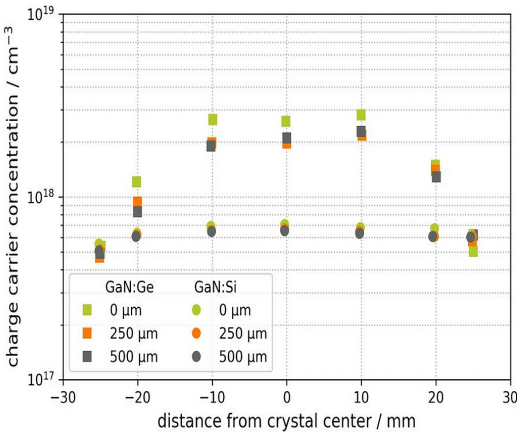


Fig. 3: Charge carrier concentration of GaN:Ge (squares) and GaN:Si (dots) measured parallel and perpendicular to the growth direction.

Since 2011 NaMLab is belonging to a small but elite group of bulk-GaN growers. It is cooperating onsite with Freiberger Compound Materials (FCM) in Freiberg and owns a modified and optimized state-of-the-art vertical HVPE reactor. The main focus of the research and development is the growth of several millimeters thick GaN crystals (Fig. 1 and 2). So far, crack-free 2“ crystals can be reliably grown. Besides scaling, the optimization of the lattice properties, e.g. the lattice bow, and the electrical properties, which range between n-type and semi-insulating, is of major scientific interest.

The latter is achieved by intentional doping, i.e. to enhance the n-type character or to suppress the unintentional doping (“UID” with charge carrier concentrations lower than 5 x 10^{16} cm^{-3}), that is inevitably present after growth. Here, the vertical HVPE reactor has four different possibilities for introducing a variety of dopants ranging from solid-state dopants to various gaseous precursors which have been investigated thoroughly in the last years.

To achieve a distinct n-type conduction, mainly silicon (Si) and germanium (Ge) were used. A gaseous dopant is utilized for Si, while a solid state method can also be applied for Ge.Here, solid germanium is introduced to the reactor and an in-situ chemical reaction is used to form a gaseous chemical compound. This involved growing n-type GaN:Ge crystals, which was confirmed by SIMS and room-temperature Hall measurements. A closer investigation of the dopant incorporation reveals an improved lateral distribution of the dopant along the crystal surface, with the doping concentration oscillating perpendicular to the investigated growth direction.

The introduction of a bubbler setup also allowed Ge incorporation via $GeCl_4$ which provides a improved control on the doping concentration. With this, higher charge carrier concentrations in the range of 2 x 10^{18} cm^{-3}, compared to Si with around 8 x 10^{17} cm^{-3}, could be achieved. In both cases, the distribution of the charge carrier concentration perpendicular to the crystal surface is very uniform. The distribution parallel to the surface is more inhomogeneous for Ge-doped than for Si-doped GaN (Fig 3). In the future the uniformity improvements for Ge doping will be of particular interest since higher charge carrier concentrations can be achieved for this dopant.

Other doping methods like doping with metal organic precursors or soluble solids in a liquid gallium source to achieve semi-insulating GaN:Fe via Cp_2Fe (ferrocene) or GaN:Mn via solid Mn have been established and investigated.

The doped crystals are also monitored with respect to their lattice and mechanical properties in order to investigate the influence of the dopants.

Cooperation: Freiberger Compound Materials GmbH, Freiberg (Germany)

Publications: J13, T2, DGKK-Workshop 06.12.2019 Dresden

Contact: Dr. Sven Jachalke

Gallium Nitride MBE & Fundamentals

During the past years ultra-pure GaN/AlGaN heterostructures with atomically-smooth interfaces and surfaces were grown by molecular beam epitaxy (MBE). The resulting layer stacks are a test ground for novel electrical and optical device concepts as well as fundamental material investigations. As a first example for fundamental material investigations, low-temperature photoluminescence (PL) spectra of ultra-pure GaN grown on dislocation-lean GaN substrates exhibit record-breaking narrow excitonic line widths and indicate the absence of unintentional impurity incorporation, except oxygen at an irreducible level of 2 x 10^{16} cm^{-3} (Fig. 1). Such pure GaN material is a perfect reference to understand PL signatures of intentionally incorporated elements (dopants), which helped to reveal the absence of any spectroscopic features associated with the potential p-type dopant carbon for decades.

Special effort was dedicated to heterostructures hosting 2-dimensional electron gases (2DEGs) at AlGaN/GaN interfaces. These 2DEGs are not only a prerequisite for the operation of lateral field-effect transistors, but also possess unique properties such as a high electron effective mass and a large g-factor. These allow to probe quantum properties in a previously inaccessible regime in mesoscopic physics. For the first time, microwave (mw) absorption could be detected within the quantum Hall regime of a 2DEG confined in a GaN/AlGaN heterostructure. The mw frequency is directly linked to the magnetic field, where the resistance change appears. In principal such a device could be used as a frequency-sensitive mw detector. On the other hand, by knowing the mw frequency these experiments allow for an accurate determination of the electron g-factor. The value for this fundamental material parameter was determined to be close to the free-electron value of 2 (Fig. 2).

Another fundamental material property is the effective electron mass. In a perpendicular magnetic field the 2D density of states splits into Landau levels, which separation is proportional to the effective mass. This modified density of states is the origin of Shubnikov-de Haas oscillations in the longitudinal resistance as well as the quantization of the Hall voltage (quantum Hall effect). Here and also for the first time, Landau level splitting in MBE-grown GaN/AlGaN heterostructures was observed optically. The reconstructed Landau level fan finally allows for a direct verification of the effective electron mass value of 0.24m_e (Fig. 3).

Cooperation: Max-Planck-Institute for Chemical Physics of Solids Dresden (Germany), Russian Academy of Sciences, Moscow (Russia), TU Dresden (IHM) (Germany), RWTH Aachen (Germany)

Publications: J8, J9, J26, J49, J51, J54

Contact: Dr. Stefan Schmult

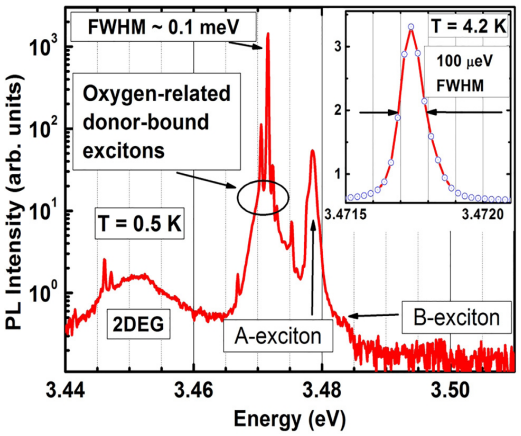


Fig. 1: Low-temperature PL spectra of ultra-pure, dislocation-lean GaN indicate the absence of unintentional impurities and exhibit record-breaking narrow excitonic line widths (inset).

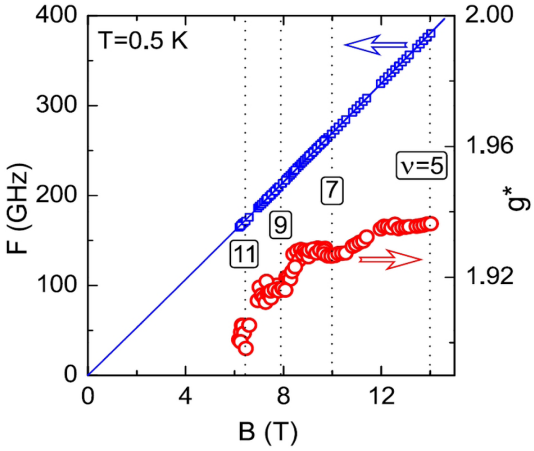


Fig. 2: Microwave frequency detection vs. magnetic field in a GaN/AlGaN heterostructure grown by MBE. These measurements allow for a direct determination of the electron g-factor, which was found to be close to the free-electron value.

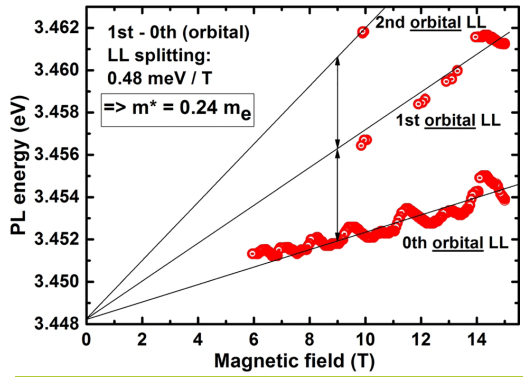


Fig. 3: Landau fan reconstructed from optically-detected Landau level splitting in a GaN/AlGaN 2DEG exposed to a perpendicular magnetic field. From the separation of the individual branches an effective electron mass of 0.24m_e was extracted.

Gallium Nitride Based Device Technology

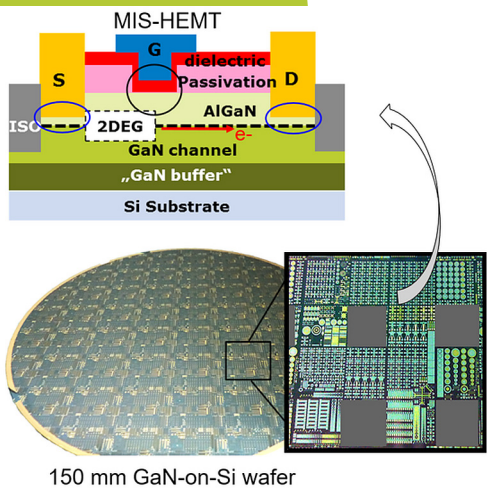


Fig. 1: Cross section MIS-HEMT device, process modules under investigation marked with circles. Below: image of processed 150 mm GaN-on-Si HEMT wafer with zoom in test chip die.

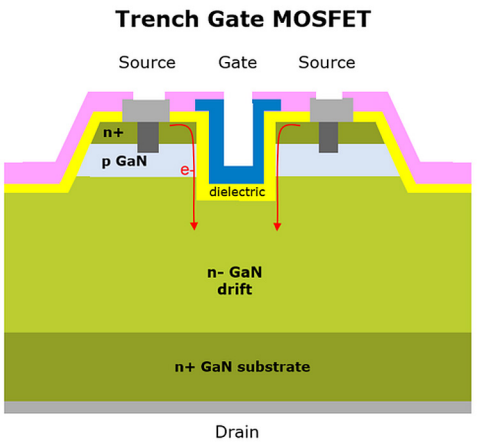


Fig. 2: Cross section vertical MOSFET with trench gate configuration in GaN matrix and backside drain contact. Device channel is formed at vertical trench sidewall along p-GaN.

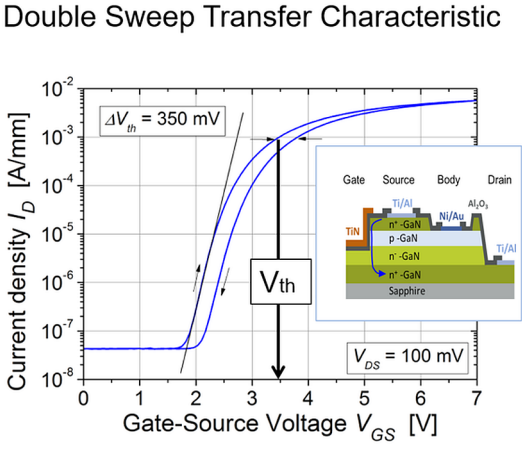


Fig. 3: Transfer characteristic of pseudo-vertical MOSFET at V_{DS} = 0.1 V. Drain current scaled on channel width in trench gate. True normally-off device operation with threshold voltage of 3.5 V is demonstrated.

The III-V compound semiconductor gallium nitride (GaN) has outstanding intrinsic material properties for power device applications. The NaMLab GaN device development is focused on electronic power devices with high voltage operation. The High-Electron-Mobility-Transistor (HEMT) concept features a 2-dimensional electron gas (2DEG) at the Al_xGa_yN/GaN heterojunction interface. It represents the backbone of GaN power transistors with planar or lateral current conduction close to the wafer surface. The material for industrial fabrication consists primarily of MOCVD grown GaN on Si(111) substrates with diameter of 150 mm or 200 mm.

A basic HEMT technology based on contact lithography for 150 mm wafer is utilized for material characterization in cooperation with external partners (Fig. 1). NaMLab is also working on process modules for improving overall device performance, stability and reliability. Related to the gate module, we investigate the integration of a high-k dielectric material underneath the gate electrode to fabricate a Metal-Insulator-Semiconductor (MIS)-HEMT. Compared to Schottky Gate HEMTs, MIS-HEMTs have the advantage of much lower gate leakage, but charge trapping effects at the dielectric/GaN interface have to be minimized for mature device operation. The second development is related to an alternative ohmic contact module based on Ta/Al metal bilayers compared to the mainstream Ti/Al contacts. Material engineering resulted in Ta/Al/TiN-ohmic contacts with low resistivity at much lower annealing temperatures (≤ 600 °C), which are gold-free and enable a higher integration flexibility.

Another device development path is related to vertical GaN power devices, having the advantage of an almost area-independent scaling of the breakdown voltage. NaMLab is developing vertical GaN MOSFET devices with trench gate configuration and device channel along the vertical sidewall of the trench (Fig. 2). The device processing technology was first implemented on pseudo-vertical devices due to better material availability. Device functionality with threshold voltage in an appropriate range (V_{TH} > 3 V) could be demonstrated and process improvement reduced charge trapping at the gate channel interface and increased the carrier mobility and current drive (Fig. 3). For increasing high voltage blocking capability (> 600 V), the technology is currently transferred from pseudo- to true vertical technology with backside contact on 2-inch free-standing GaN substrates with larger drift layer thickness. Besides further module development, the focus on device level shifts from single trench cell test devices to power demo-devices with multiple gate trenches connected in parallel.

Cooperation: Freiberger Compound Materials GmbH, Freiberg (Germany), TU Dresden (IHM) (Germany), TU-BA Freiberg (Germany), RWTH Aachen (Germany), X-FAB (Germany)

Publications: J8, J9, J32

Contact: Dr. Andre Wachowiak

Versatile Passivation Layers For Silicon Solar Cells

Highly efficient silicon solar cells require excellent surface passivation. Al_2O_3 is now the standard material for p-type silicon as high-quality passivation. At NaMLab, homogeneous Al_2O_3 layers were further developed to multi-oxide nanolaminates with tailored material properties. These layers enhance the classical surface passivation and open the field of conductive passivation for next generation PERC (Passivated Emitter and Rear Contact) cells.

(I) *Classical passivation*: engineering of interface charge carriers. Various types of dielectrics tend to form different amounts of fixed charges at the interface. Al_2O_3 contains negative fixed charges with a density in the order of 10^{12} cm^{-2}, while the number of fixed charges in HfO_2 is one order of magnitude lower. SiO_2 exhibits a similar density as the one for Al_2O_3, despite this they are of positive nature. One can make use of these particular features. By employing multi-oxide stacks, it is possible to influence the number of charges, which effectively act at the interface to Silicon. Fig. 1 shows the adjustability of the fixed charges between 3 x 10^{12} cm^{-2} and almost zero by adding a thin interfacial layer of HfO_2. A SiO_2 interface goes a step beyond. It offers the option to change the type of the fixed charges from a negative to a positive value continuously. Fig. 2 shows an example of an Al_2O_3/HfO_2 nanolaminate.

(II) *Conductive passivation*: The next step towards advanced PERC cells is the introduction of a conductive surface passivation. There are two major advantages. On the one hand, opening the classical passivation layer in order to contact the cell itself involves process steps, which consume high amounts of energy. These process steps would be obsolete. On the other hand, losses attributed to the lateral diffusion of charge carriers towards the local contact openings and recombination of charge carriers at the openings itself will be reduced. Therefore, the efficiency of the cell will be increased. There are four major criteria to be fulfilled. The contacts have to exhibit a very high transparency for visible light, a good passivation behavior, a good conductivity and need to be compatible to the existing PERC process flow (see Fig. 3). Since 2016 NaMLab is investigating oxide layer stacks as potential candidates for this purpose. The main concept consists of a passivating tunnel oxide (Al_2O_3) with thicknesses below 1 nm and a transparent conducting oxide (doped TiO_x). Therefore, the result is an enhancement of the highly passivating Al_2O_3 developed at NaMLab previously.

The applied atomic layer deposition technique provides highly accurate growth control in the sub-nm range. It opens the possibility to tailor material properties of Al_2O_3-based nanolaminates for novel functionality in future solar cell concepts.

Cooperation: TU Dresden (IHM) (Germany), FAP GmbH, Dresden (Germany), Meyer Burger AG, Hohenstein-Ernstthal (Germany)

Publications: C14, C17

Contact: Dr. Matthias Grube

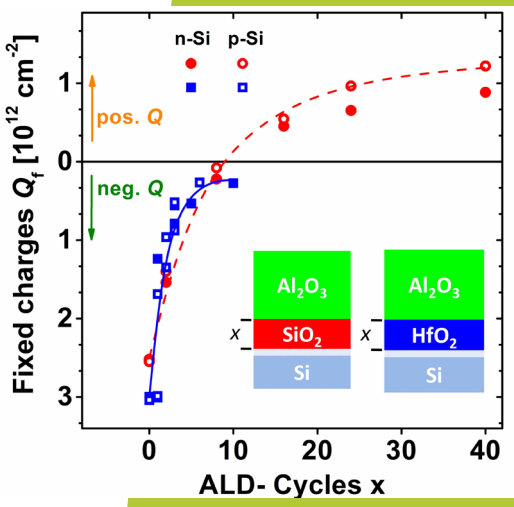


Fig. 1: Measured effective density of fixed charge carriers in n- and p-type Si passivated with Al_2O_3 and a thin interface layer of HfO_2 or SiO_2

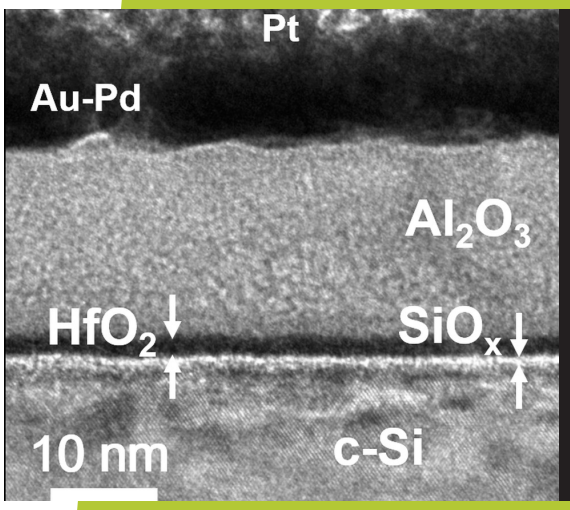


Fig. 2: Image of a HfO_2/Al_2O_3 nanolaminate recorded by Transmission Electron Microscopy.

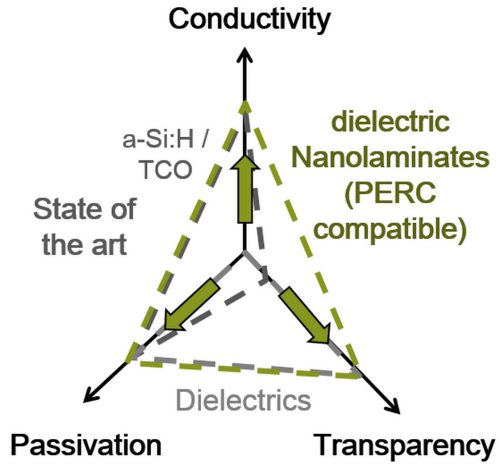


Fig. 3: "Magical triangle" of conducting passivation of solar cells. Besides the mandatory compatibility to the PERC production process, high conductivity, high transparency and a very good passivation are the main requirements.

Competences

High resolution SEM imaging of heterostructures.

Electrical Characterization

Electrical measurements are essential for the characterization of the materials that are used to create electronic devices and circuits. NaMLab adopts a broad spectrum of electrical measurement techniques and analysis methods for device characterization. This includes capacitance measurements, such as C(V), C(T) and C(f), current measurements with down to femtoampere resolution at temperatures between 5 K and 450 K and voltages up to 3000 V. Samples can be analyzed by direct probing on wafer level using single probes, probe cards or special RF-probes. Package level testing can be performed for long-term reliability characterization or for the adoption of our devices in test-circuits. In addition, carrier lifetime measurements are available on substrates with microwave-detected photoconductivity.

The established methods at NaMLab include:

- Analysis of single memory cells (memory window, retention, endurance,...) by static and pulsed measurements
- Determination of transistor and capacitor characteristic curves by C-V and I-V measurements
- Determination of sheet resistance for thin layers.
- Determination of doping profiles by scanning spreading resistance Microscopy (SSRM)
- Reliability characterization of dielectric and transistors
- Defect characterization by charge pumping and charge trapping analysis and defect spectroscopy
- Measurement of charge carrier mobility with Hall and split-C(V)
- Pulsed and high frequency measurements
- Power device characterization

Electrical material characterization such as the four point probe measurement is regularly used to attain fast feedback loops, thus supporting the material development (Fig. 1).

Besides the utilization of standard single device measurements, customized characterization setups are created at NaMLab. This work includes the development of special circuits that are mandatory to control non-standard test environments. Fig. 2 shows such an adaptive level-shifter circuit used for the digital control of a memory test array. The investigation of a novel memory device concept required the adaption of the operation voltage of the complete memory chip including the I/O voltages in order to optimize the operation conditions of the novel devices under test.

In Fig. 3 the measured bit-map of one quarter of a 64kBit memory array is shown. This measurement was performed in order to characterize the top-metallization layer which was manufactured at NaMLab on top of a 28 nm CMOS test chip.

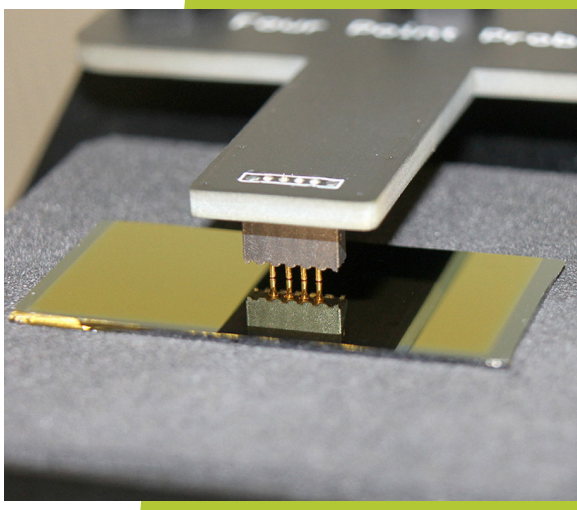


Fig. 1: Four point probe measurement setup for electrical characterization of thin films.

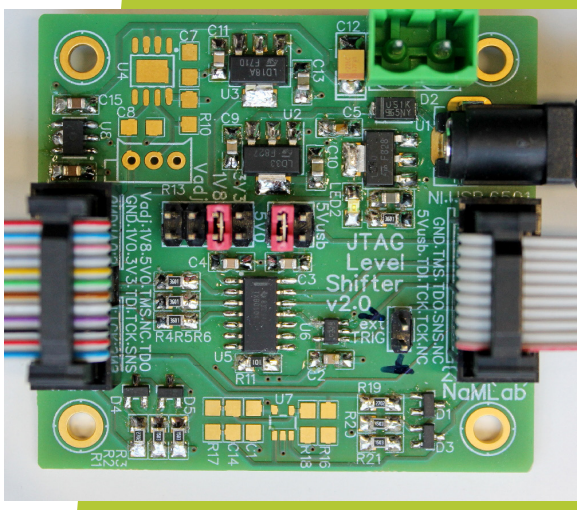


Fig. 2: Circuit for JTAG control under variable voltage conditions that was developed at NaMLab to control a resistive RAM memory array.

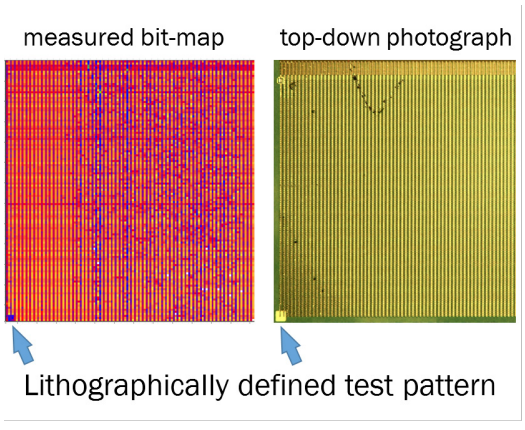


Fig. 3: Measured bit-map of a quarter of a 64kbit resistive RAM array. Special lithographically structured test patterns are used for verification of the digital addressing scheme of the chip.

Contact: Dr. Stefan Slesazeck

Physical Characterization

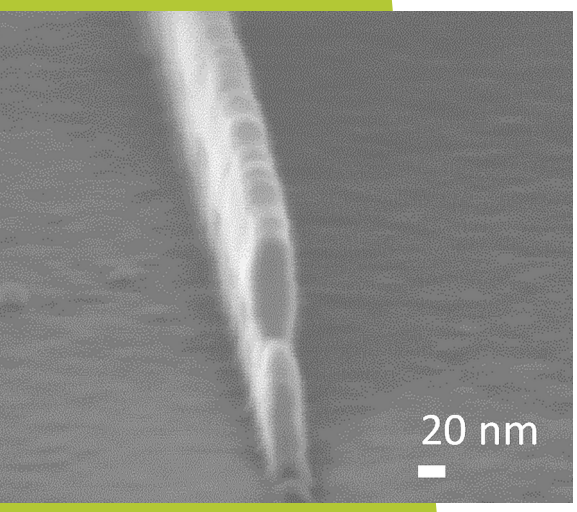


Fig. 1: SEM image of standing silicon fin fabricated on an SOI substrate with hardmask after RIE etching, “bird‘s view”.

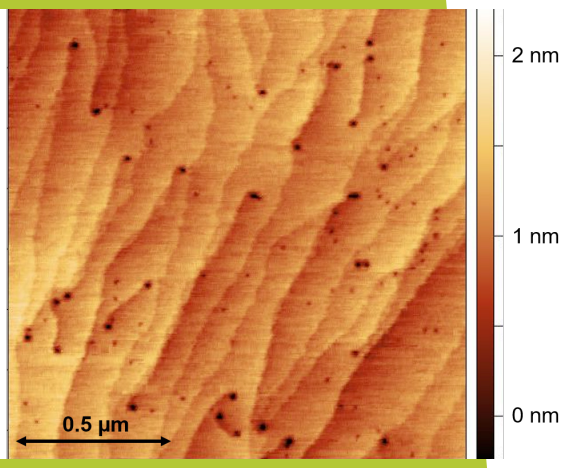


Fig. 2: Surface topography of MOCVD GaN with monolayer stepped terrace structure. Pits of shallow (deeper) depth indicate end points of threading edge (screw + mixed) dislocations.

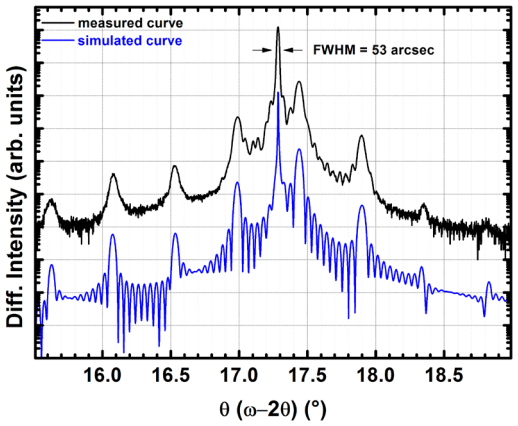


Fig. 3: Measured and simulated high resolution X-ray diffraction pattern of AlGaN/GaN superlattices grown by molecular beam epitaxy at NaMLab.

NaMLab engages in state-of-the-art material research for nanoscale applications in strong co-operation with its industry partners as well as with other laboratories to foster progress in industry oriented as well as basic research. The focus of physical characterization at NaMLab can be summarized as follows: The available high-resolution scanning electron microscope (HRSEM) is capable of providing high magnification images down to 2 nm resolution (Fig. 1). Besides top-view images, cross-sectional SEM imaging showing the entire layer architecture (in case of thin multilayer film structures) can be imaged easily by a switch of sample holders. Furthermore, the SEM is equipped with an EDX (energy dispersive) detector. A very accurate and trustworthy chemical composition determination of the samples is possible covering almost the entire periodic table. Another equally fascinating feature of HRSEM is the high resolution electron beam lithography (e-beam) for structuring e-beam resist with accuracy in the 15 nm regime.

The atomic force microscope (AFM) is equipped with the Nanoscope user interface for measurement and data analysis. Resolution in the order of 2 nm in the scanning direction and below 0.1 nm perpendicular to the scanning direction is routinely realized in mapping the surface topography. An example of an epitaxial grown GaN surface is shown in Fig. 2. The AFM can be operated in the conductive AFM (C-AFM) mode and in the mode of Scanning Spreading Resistance Microscopy (SSRM). C-AFM is used to investigate the local leakage current density of thin dielectric layers, SSRM is applied to map the spatial dopant distribution of two-dimensional cross-sectional structures in semiconductors. A special method for analyzing piezoelectric materials is the piezo force microscopy (PFM). In this method the vertical displacement of the AFM tip is measured in response to an electrical excitation of the sample. The PFM method is currently refined for the analysis of the ferroelectric switching behavior of thin films.

X-ray diffraction (XRD): A multifunctional diffractometer allows high resolution X-ray diffraction, X ray diffraction in classical Bragg-Brentano set-up, grazing incidence diffraction and X-ray reflectivity as well as reciprocal space mapping and polefigure measurements in the same apparatus. The tool has a resolution of < 40 arcsec and is used for phase analysis, measuring reciprocal space maps,determining the composition of alloys, layer thickness and stress state. A high resolution X-ray diffraction measurement on an AlGaN/GaN superlattice structure is shown in Fig. 3.

Contact: Dr. Andre Wachowiak

Optical Characterization

A key method in understanding fundamental semiconductor material properties and device performance is optical characterization. At NaMLab, various techniques such as photoluminescence (PL, Fig. 1), Raman and Fourier transform infrared spectroscopy are applied to determine defect types and energies, phonon energies and transmission and reflection characteristics in semiconductor materials. Furthermore, photoactive electrical devices can be characterized.

Special focus of NaMLab's optical activities over the past two years was placed on low-temperature PL measurements of gallium nitride (GaN) material with its band gap of 3.4 eV. The HeCd excitation laser emitting at 325 nm had to be refurbished after reaching the end of its lifetime and now features an output power in excess of 50 mW again. A challenge was and still is to resolve very narrow excitonic features originating from defects in epitaxial GaN. As an example, in low-temperature PL spectra the oxygen-bound donor exciton has been resolved with a record-breaking line width of ~ 150 µeV (Fig. 2) demonstrating both, the outstanding sample properties and the capability of the PL set-up.

With the Raman set-up, degradation mechanisms of silicon nanowire anodes integrated in lithium ion batteries could be extensively investigated in situ during Si lithiation/delithiation. With these measurements a relationship between structural and electrochemical properties over electrode cycling could be established. As a result, amorphous as well as liquid and transient species in a battery cell were observed and the difference between silicon nanowires and its carbon-coated counterpart as anode materials became immediately visible (Fig. 3).

In summary, established optical methods at NaMLab include:

- Low-temperature photoluminescence (15 - 300 K) in the UV – visible spectral range (340 nm - 800 nm) with UV (325 nm) laser excitation
- Spectral response with and without bias illumination for photosensors and solar cells
- Micro-Raman mapping with 457, 514 and 785 nm excitation wavelength (spatial resolution: 1 µm) for e.g. local strain analysis
- IR and VIS-NIR ellipsometry and VIS-NIR reflectometry
- Microwave detected photoconductivity for 2D mapping of minority carrier lifetimes in silicon
- Fourier Transform Infrared (FTIR) Spectroscopy (2000 - 20000 nm) for analyzing lattice and molecular vibrational bands

Publications: J40, J49, J54

Contact: Dr. Matthias Grube, Dr. Stefan Schmult

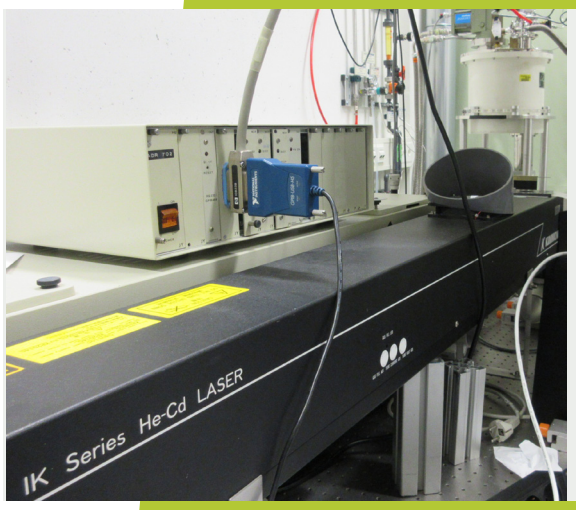


Fig. 1: Low-temperature photo-luminescence set-up with a refurbished KIMMON HeCd UV excitation laser.

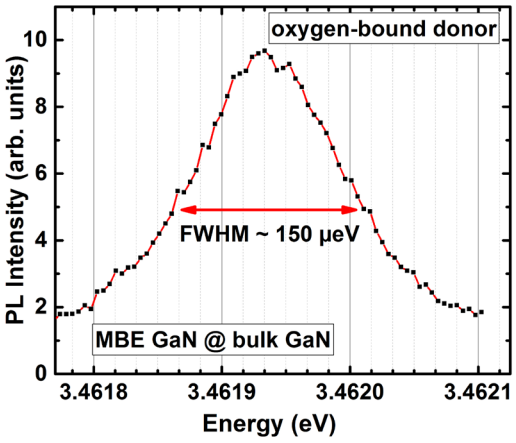


Fig. 2: Highly-resolved photo-luminescence signature with 150 µeV line width of the oxygen-bound donor in a 1 µm thick ultra-pure GaN layer grown by MBE on a bulk GaN template.

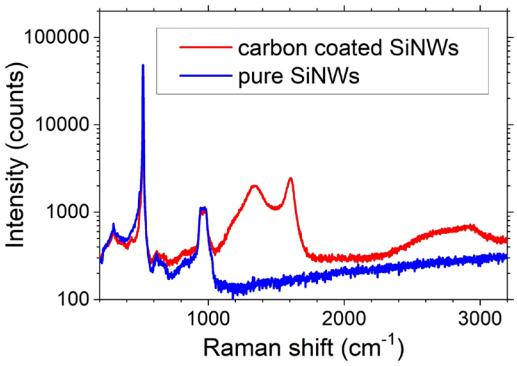


Fig. 3: Raman data obtained in NaMLab's optical lab reveal straight-forward different signatures for various battery anode materials and allow to characterize in-situ degradation processes of these materials.

Device Reliability

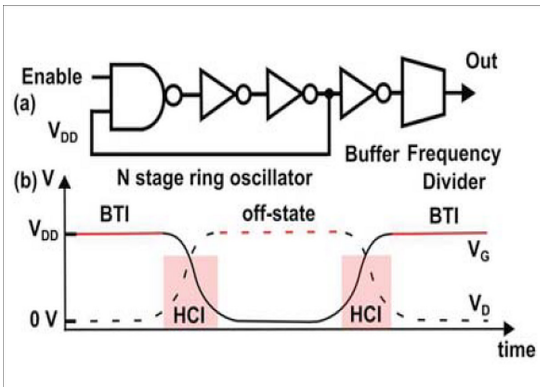


Fig. 1: Schematic of ring oscillator test structure and voltage evolution during dynamic stress indicating the off-state stress condition.

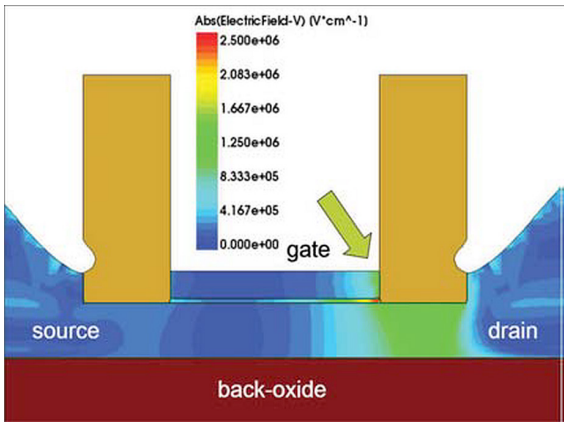


Fig. 2: TCAD simulation of the electric field distribution within a 22nm FDSOI transistor under off-state stress condition. Field peaks at the drain-side during off-state stress can lead to asymmetric device degradation.

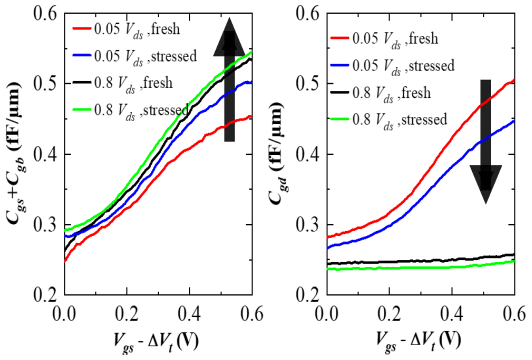


Fig. 3: From S-Parameter measurements extracted gate capacitance to source, drain and bulk (C_{gs}, C_{gd}, C_{gb}) after HCI stress reveals asymmetric device degradation.

The development of novel microelectronic devices as well as the scaling of existing devices concepts is tightly linked to the availability of mature and reliable integration of new dielectrics. On the nanometer scale those materials act as gate insulator, stress or strain layers or memory dielectrics. NaMLab performs electrical stress measurements on a large variety of devices to assess the reliability of the used dielectric materials. Moreover, simulation and modeling of the different degradation effects give deeper insight into the physical mechanisms. The results of the spatial localization of different defect sites within the devices provides an informative base to our partners for the optimization of manufacturing processes or device structures while targeting at further improved reliability.

In face of the increasing complexity of power devices or high performance logic devices any compromise in reliability is not acceptable. Especially for high dielectric constant gate insulators, the fundamental understanding of bias temperature instability (BTI), hot carrier injection (HCI), stress induced leakage currents (SILC), and time dependent dielectric breakdown (TDDB) are of major interest. To further deepen the understanding of use-case realistic stress conditions we put additional focus on the assessment of circuit reliability. That is, besides the standard reliability tests on single devices that are typically performed with high statistics at our partners premises, more advanced and time consuming characterization methods are investigated at NaMLab.

Fig. 1 depicts the schematic of a ring-oscillator circuit where stress conditions switch between BTI, HCI and an off-state stress at high frequencies close to use-conditions. Our measurement results show, that the off-state stress occurring at the drain-side of the transistors (when the gate voltage is low while drain voltage is high) leads to a modified degradation mechanism. The reason behind asymmetric device degradation is a negative field peak at the drain-sided channel edge (see Fig. 2). The trapping induced by this field peak induces a local threshold voltage shift at the drain side counteracting the BTI degradation in the on-state. Consequently, the measured frequency degradation in the ring oscillator is lower than extrapolated by pure DC BTI stress analysis.

The growing interest in high speed and RF technologies assert for the importance of reliability characterization beyond the conventional DC or AC methodology. Power amplifiers for example that are adopted to realize on-chip transmitters have to operate stable at frequencies well beyond the GHz range. Thus, the correct understanding of degradation mechanisms that affect the RF device parameters becomes increasingly important. The data shown in Fig. 3 reveal changes in the effective gate to drain and gate to source capacitance (C_{gd}, C_{gs}) that is caused by an asymmetric threshold voltage shift under HCI stress conditions.

Publications: C15, C19, T4

Contact: Dr. Stefan Slesazeck

Sample Preparation

The research programs at NaMLab typically require very specific preparation of samples. This preparation can include deposition of thin films and layers, thermal treatment of samples, patterning by lithography and etching, as well as sample cutting, grinding, polishing and engravings. For this purpose, the 330 m² cleanroom facility includes various types of deposition tools: physical vapor deposition (PVD), atomic layer deposition (ALD), chemical vapor deposition (CVD), and molecular beam epitaxy (MBE). Post deposition anneals can be performed in various hot and cold wall ovens, which cover a temperature range for room temperature up to 1200 °C. There are fast ramping Rapid Thermal Processing machines available as well as furnaces for long-term treatment. Structures in the range of micro- and nanometers can be manufactured by employing shadow masking and lithographic methods like electron beam and laser lithography. The removal of the material includes wet chemical and reactive ion etching (RIE).

Additional requirements of the scientific processing is adapting wafer geometries, chip dicing and creation of process compatible gadgets e.g. for sample handling. Therefore, NaMLab provides several tools to meet these requirements.

A Synova LSC 300 W Laser cutter (Fig. 1) is located in NaMLabs clean room. A Laser (λ = 532 nm) beam is guided by a water jet of 50 µm in diameter, which additionally cools the sample during the cutting process. It offers the possibility to process wafers with diameters up to 300 mm and substrate thicknesses up to 1 mm. Via a CNC based vacuum chuck any shape can be produced as well as wafer recess and surface roughening is possible. This technique is used for dicing silicon wafers or cutting small pieces without destroying processed and reusable wafers.

In order to prepare the produced layer stacks and device structures for the analysis by scanning electron microscopy or atomic force microscopy, NaMLab uses a Bühler MetaServ250 chemical-mechanical polishing tool for smoothening previously cut or broken sample edges. In addition, high-precise cross sections and the removal of individual layers is possible with the aid of special polishing rags and suspensions. For cleaning and wet chemical treatment (Fig. 2) of samples, NaMLab owns four wet benches equipped with overflow basins. They are located in a DIN ISO 5 cleanroom. Ultra and mega sonic tools for mechanical supported surface cleaning in deionized water are in operation. Also cleaning steps like RCA clean and selective material etching can be performed.

For sample preparation and combined surface analysis in the micro and nanometer range, NaMLab uses a FEI Expida 1285 Focused Ion Beam (FIB) system. The gallium ion beam current can be set be-tween 1 pA and 30 nA. Cross section formation and milling of TEM lamellas are scopes of application as well as localized removal and deposition of material. Samples can be in-situ covered with protecting or decorating layers via several gas inlets.

Fig. 1: Laser cutter tool for wafer cutting and engraving: Synova LSC 300W.

Fig. 2: Various possibilities to perform controlled wet chemical and reactive ion etching.

Fig. 3: a) FEI Expida 1285 Focused Ion Beam (FIB) system and b) SEM image of a FIB milled transistor cross section.

Contact: Dr. Matthias Grube

Facts & Figures

NaMLab main building.

NaMLab In Numbers

Annual Budget

The annual budget over the past six years reflects that NaMLab gGmbH has been established as an institute with full operation. Any further growth of the research institute is limited by the available office space. The turnover is stable at about 3.5 Mio. Euros. The budget of the publicly funded projects decreased over past five years. In parallel, contract research increased by the same amount. Both indicate a change in quality of research. Publicly funded research results are transferred to industrial partners and industry uses the capabilities of NaMLab for research. The basic financial support has reached a basic rate and increased slightly starting in 2017. The basic financial support accounted to about 15% to 20% of the overall revenue.

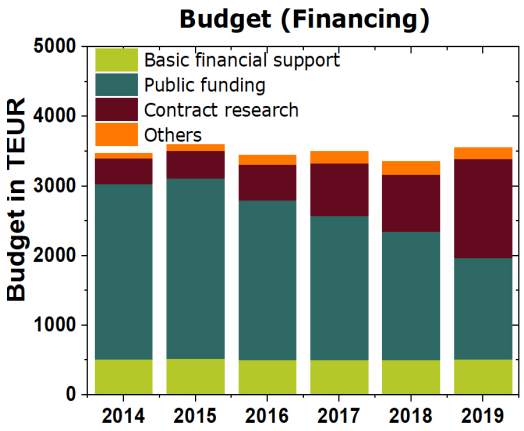


Fig. 1: Annual budget.

Investment Budget

The cleanroom facility at NaMLab conforms to the highest standards. 250 m² of class 6 and 50 m² of class 5 clean room (EN ISO 14644) are available for experimental work. With its core competency in materials development, NaMLab runs several deposition technologies such as evaporation, molecular beam epitaxy, sputtering, chemical vapor deposition and atomic layer deposition. In total thirteen processing tools are used for research work. A wet chemistry area is equipped with cleaning, etching and spin coating processes. Two state-of-the-art electrical characterization labs for material and device characterization are equipped with 200 and 300 mm probe stations. Additional labs for optical and physical characterization are available. Furthermore NaMLab rents a lab located in Freiberg, a city close to Dresden, hosting a Hydride Vapour Phase Deposition tool for research on GaN crystal growth. The main investment in 2018 and 2019 has been a laser lithography system for flexible processing of small samples and easier combining of micrometer-sized structures with electron beam-patterned structures. Therefore the wet chemistry area was rearranged into a yellow-light area. The new equipment was financed by the basic financial support of the Free State of Saxony out of the budget approved by the Saxon State Parliament. Additionally NaMLab has invested in smaller upgrades of deposition tools and IT hardware and software.

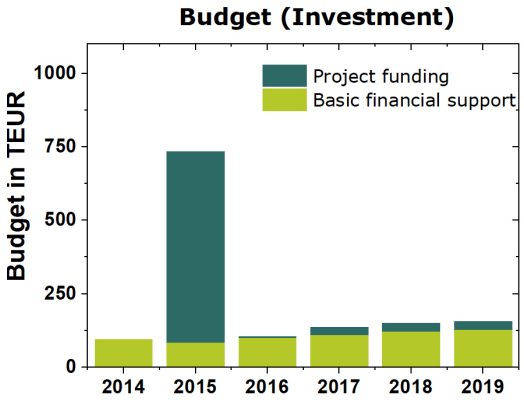


Fig. 2: Investment budget.

Employment Development

In 2018/2019, the number of employees has been stable. End of 2019 the total staff counted 42 members. This includes 4 employees for administration, three employees for technical support, 4 senior scientists and 4 student assistants. Technicians and senior scientist guarantee an excellent and stable scientific and technical know-how basis on semiconductor devices, technology and materials for running and future projects. Currently, 14 scientists are planning to submit a PhD thesis. Additionally, the number of master theses, project works and semester works increased significantly over the last two years.

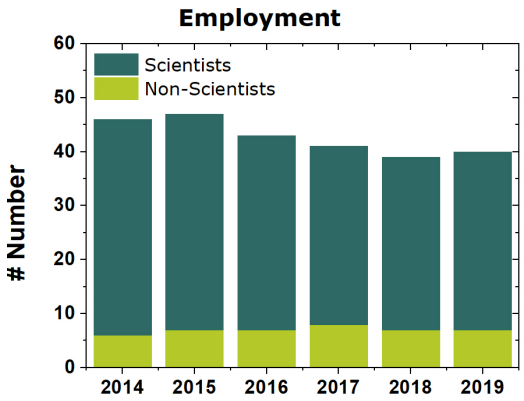


Fig. 3: Employee number development.

Contact: Dr. Alexander Ruf

Projects

Europäische Union

HERALD (16866)

Hooking together European research in atomic layer deposition

3eFERRO (708302)

Energy Efficient Embedded Non-volatile Memory Logic based on Ferroelectric Hf(Zr)O2

Bundesministerium für Wirtschaft und Energie

Tibet (03SF0538A)

Transparent, conductive and passivating electrodes for high-efficient solar cells

Enkrist (03ET1398B)

Energy saving by the availability of better and cost-efficient carbide and nitride semiconductor crystals

Bundesministerium für Bildung und Forschung

BamoSa (03X4637E)

WING center: Battery-mobility in Saxony

GaNESIS (16ES1090)

AlN/GaN epitaxy on silicon using reactive plus magnetron sputtering

KaSiLi (03XP0254C)

In-situ Raman investigations on anodic protective layers of silicon- and lithium-based anode materials

Europäische Union

Bundesministerium für Bildung und Forschung

EleGaNT (100201538)

Development of freestanding substrates for vertical GaN transistors

Phoenix (100274129)

Phenomena and technologies of new highly energy-efficient non-volatile memories

EFFSIL300 (100316972)

Efficient and safe power transistors based on 300 mm wafers

F-GaN (100336682)

Development of a reliable and robust foundry process technology for GaN devices based on 200 mm epitaxial GaN on silicon wafers

GaNHoch-VFT (100364091)

Equipment GaN on GaN high voltage and high frequency transistors development

This measure is financed by the Saxon State government out of the State budget approved by the Saxon State Parliament.

Projects

ReproNano (WE 4853/1-3)

Reconfigurable silicon nanowire based logic circuits

Inferox (MI 1247/11-2)

Incipient ferroelectrics on the basis of hafnium oxide

LAMP (MI 1247/12-1/2)

Locally Active Memristive Data Processing

CfAED (EX1056/2)

Center for Advancing Electronics Dresden

HiMGaN (MI 1247/15-1)

Exploration of novel electrical and electro-optical device concepts and fundamental physical effects in high-quality wide-band-gap semiconductor heterostructures

Bundesministerium für Bildung und Forschung

DFG

Ecsel Powerbase (662133/16ESE0005S)

Enhanced substrates and GaN pilot lines enabling compact power applications

Ecsel UltimateGaN (826392/16ESE0422S)

Research for GaN technologies, devices and applications to address the challenges of the future GaN roadmap

ECSEL Joint Undertaking

Bundesministerium für Bildung und Forschung

Freistaat Sachsen

This measure is financed by the Saxon State government out of the State budget approved by the Saxon State Parliament.

Alexander von Humboldt Foundation Postdoktorand (Ref. 3.5 - KOR / 1161292)

Alexander von Humboldt research scholarship

Dr. Min Hyuk Park

Alexander von Humboldt Stiftung/Foundation

Falcon (ZF4737101AG9)

Flash lamp based activation of passivating contacts for highly efficient solar cells

Gefördert durch:

Bundesministerium für Wirtschaft und Energie

aufgrund eines Beschlusses des Deutschen Bundestages

ZIM Zentrales Innovationsprogramm Mittelstand

NaMLab Goes Public

Fig. 1: In the long night of science, people meet NaMLab and get inspired by nano-electronic science and a beautiful evening.

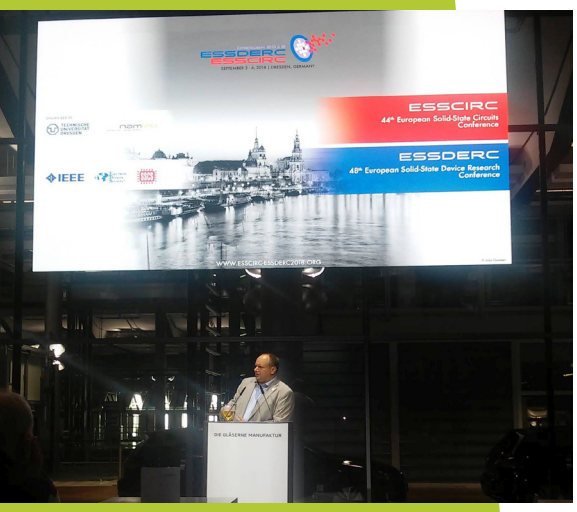


Fig. 2: At ESSDERC & ESSCIRC 2018, about 600 scientist from 33 countries met for an exciting event.

Fig. 3: Annual workshop of DGKK 2019 welcomed 115 participants from 5 countries.

In 2018 and 2019, NaMLab continued its efforts to make scientific research on nanoelectronic materials, devices and application more accessible for the public in general. In particular, it kept its efforts to inspire young people studying science or engineering. NaMLab took part in many joined activities like the “Long Night of Science”, the summer school “Dresden Microelectronics Academy”, and the “University Day” of the Technical University Dresden. Additionally the researchers of NaMLab participated as supervisor of the annual work experience in 7th and 8th school class of the Martin-Andersen-Nexö secondary school Dresden.

Long Night of Science 2018

On June 15, 2018, research institutes, companies, and four universities opened their laboratories, lecture halls and offered a comprehensive program for the 16th Long Night of Science. At NaMLab the people got acquainted with material research for future electronics. The program offered visiting tours through the laboratories and presented typical characterization methods in experimental shows.

ESSDERC & ESSCIRC 2018

The 48th European Solid-State Device Research Conference ESSDERC and the 44th European Solid-State Circuits Conference ESSCIRC from September 3 - 6, 2018 has been organized by the chair of Nanoelectronic Materials of TU Dresden and NaMLab gGmbH. More than 600 scientists from 33 countries met for an exciting event and examined technology, circuit design and industrial trends.

Novel High-k Application Workshop 2018/2019

Supported NaMLab the Novel High-k Application Workshop 2018 was organized by the University of Wrocław, Poland. In March 2019 NaMLab invited to the Novel High-k Application Workshop in Dres-den again. New challenges offered by the application of high-k dielectric materials in micro- and nanoelectronics have been dis-cussed by more than 80 participants from industry, research institutes and universities. In this series of annual workshops NaMLab has created a stimulating platform for application-oriented scientists to exchange ideas and discuss latest experimental results.

Annual workshop of DGKK 2019

The annual workshop of DGKK, the German association of crystal growth on the epitaxy of III/V compounds is a two-day meeting dedicated to the growth, processing and characterization of epitaxial III/V compound materials. The 2019 workshop from December 5 - 6 was organized by the chair of Nanoelectronic Materials of TU Dresden and NaMLab gGmbH, and welcomed 115 participants from Germany, the Czech Republic, the Netherlands, Great Britain, and the United States at a beautiful venue in downtown Dresden.

NaMLab In The Media

Various press articles about research at NaMLab

Contact: Prof. Dr.-Ing. Thomas Mikolajick

Publication List 2018/2019

Journal Papers 2018-2019

J1	T. Baldauf, A. Heinzig, T. Mikolajick, and W. M. Weber, 'Vertically Integrated Reconfigurable Nanowire Arrays', IEEE Electron Device Letters, vol. 39, no. 8, pp. 1242–1245, Aug. 2018
J2	P. Buragohain et al., 'Nanoscopic studies of domain structure dynamics in ferroelectric La:HfO2 capacitors', Appl. Phys. Lett., vol. 112, no. 22, p. 222901, May 2018
J3	S. Doering, A. Wachowiak, H. Roetz, S. Eckl, and T. Mikolajick, 'SDVSRM - a new SSRM based technique featuring dynamically adjusted, scanner synchronized sample voltages for measurement of actively operated devices', Ultramicroscopy, vol. 193, pp. 24–32, Oct. 2018
J4	F. P. G. Fengler, M. Hoffmann, S. Slesazeck, T. Mikolajick, and U. Schroeder, 'On the relationship between field cycling and imprint in ferroelectric Hf0.5Zr0.5O2', Journal of Applied Physics, vol. 123, no. 20, p. 204101, May 2018
J5	F. P. G. Fengler et al., 'Analysis of Performance Instabilities of Hafnia-Based Ferroelectrics Using Modulus Spectroscopy and Thermally Stimulated Depolarization Currents', Advanced Electronic Materials, vol. 4, no. 3, p. 1700547, 2018
J6	E. D. Grimley et al., 'Insights into Texture and Phase Coexistence in Polycrystalline and Polyphasic Ferroelectric HfO2 Thin Films using 4D-STEM', Microscopy and Microanalysis, vol. 24, no. S1, pp. 184–185, Aug. 2018
J7	E. D. Grimley, T. Schenk, T. Mikolajick, U. Schroeder, and J. M. LeBeau, 'Atomic Structure of Domain and Interphase Boundaries in Ferroelectric HfO2', Advanced Materials Interfaces, vol. 5, no. 5, p. 1701258, 2018
J8	R. Hentschel, J. Gärtner, A. Wachowiak, A. Großer, T. Mikolajick, and S. Schmult, 'Surface morphology of AlGaN/GaN heterostructures grown on bulk GaN by MBE', Journal of Crystal Growth, vol. 500, pp. 1–4, Oct. 2018
J9	R. Hentschel, S. Schmult, A. Wachowiak, A. Großer, J. Gärtner, and T. Mikolajick, 'Normally-off operating GaN-based pseudovertical MOSFETs with MBE grown source region', Journal of Vacuum Science & Technology B, vol. NACMBE2018, no. 1, p. 02D109, Mar. 2018
J10	M. Hoffmann et al., 'Ferroelectric negative capacitance domain dynamics', Journal of Applied Physics, vol. 123, no. 18, p. 184101, May 2018
J11	M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, 'On the stabilization of ferroelectric negative capacitance in nanoscale devices', Nanoscale, vol. 10, no. 23, pp. 10891–10899, Jun. 2018
J12	B. Ibarlucea et al., 'Gating Hysteresis as an Indicator for Silicon Nanowire FET Biosensors', Applied Sciences, vol. 8, no. 6, p. 950, Jun. 2018
J13	S. Jachalke et al., 'Pyroelectricity of silicon-doped hafnium oxide thin films', Appl. Phys. Lett., vol. 112, no. 14, p. 142901, Apr. 2018
J14	R. Materlik, C. Künneth, M. Falkowski, T. Mikolajick, and A. Kersch, 'Al-, Y-, and La-doping effects favoring intrinsic and field induced ferroelectricity in HfO2: A first principles study', Journal of Applied Physics, vol. 123, no. 16, p. 164101, Apr. 2018
J15	B. Max, M. Pešić, S. Slesazeck, and T. Mikolajick, 'Interplay between ferroelectric and resistive switching in doped crystalline HfO2', Journal of Applied Physics, vol. 123, no. 13, p. 134102, Apr. 2018
J16	T. Mikolajick, S. Slesazeck, M. H. Park, and U. Schroeder, 'Ferroelectric hafnium oxide for ferroelectric random-access memories and ferroelectric field-effect transistors', MRS Bulletin, vol. 43, no. 5, pp. 340–346, May 2018
J17	H. Mulaosmanovic, E. Chicca, M. Bertele, T. Mikolajick, and S. Slesazeck, 'Mimicking biological neurons with a nanoscale ferroelectric transistor', Nanoscale, vol. 10, no. 46, pp. 21755–21763, Nov. 2018
J18	M. H. Park et al., 'Effect of Annealing Ferroelectric HfO2 Thin Films: In Situ, High Temperature X-Ray Diffraction', Advanced Electronic Materials, vol. 4, no. 7, p. 1800091, 2018
J19	M. H. Park et al., 'Origin of Temperature-Dependent Ferroelectricity in Si-Doped HfO2', Advanced Electronic Materials, vol. 4, no. 4, p. 1700489, 2018
J20	M. H. Park et al., 'Understanding the formation of the metastable ferroelectric phase in hafnia–zirconia solid solution thin films', Nanoscale, vol. 10, no. 2, pp. 716–725, Jan. 2018
J21	M. H. Park, Y. H. Lee, T. Mikolajick, U. Schroeder, and C. S. Hwang, 'Review and perspective on ferroelectric HfO2-based thin films for memory applications', MRS Communications, vol. 8, no. 3, pp. 795–808, Sep. 2018
J22	S. J. Park et al., 'Reconfigurable Si Nanowire Nonvolatile Transistors', Advanced Electronic Materials, vol. 4, no. 1, p. 1700399, 2018
J23	M. Pešić et al., 'Built-In Bias Generation in Anti-Ferroelectric Stacks: Methods and Device Applications', IEEE Journal of the Electron Devices Society, vol. 6, pp. 1019–1025, 2018
J24	M. Pešić, U. Schroeder, S. Slesazeck, and T. Mikolajick, 'Comparative Study of Reliability of Ferroelectric and Anti-Ferroelectric Memories', IEEE Transactions on Device and Materials Reliability, vol. 18, no. 2, pp. 154–162, Jun. 2018
J25	T. Schenk et al., 'Physical Approach to Ferroelectric Impedance Spectroscopy: The Rayleigh Element', Phys. Rev. Applied, vol. 10, no. 6, p. 064004, Dec. 2018

Journal Papers 2018-2019

J26	S. Schmult et al., 'The inherently absent 2-dimensional electron gas in ultra-pure GaN/AlGaN heterostructures', arXiv:1812.07942 [cond-mat], Dec. 2018, Accessed: Sep. 10, 2019. [Online]. Available: http://arxiv.org/abs/1812.07942.
J27	U. Schroeder et al., 'Lanthanum-Doped Hafnium Oxide: A Robust Ferroelectric Material', Inorg. Chem., vol. 57, no. 5, pp. 2752–2765, Mar. 2018
J28	A. V. Shchepetilnikov et al., 'Electron spin resonance in a 2D system at a GaN/AlGaN heterojunction', Appl. Phys. Lett., vol. 113, no. 5, p. 052102, Jul. 2018
J29	I. Stolichnov et al., 'Genuinely Ferroelectric Sub-1-Volt-Switchable Nanodomains in HfxZr(1–x)O2 Ultrathin Capacitors', ACS Appl. Mater. Interfaces, vol. 10, no. 36, pp. 30514–30521, Sep. 2018
J30	P. Buragohain et al., 'Fluid Imprint and Inertial Switching in Ferroelectric La:HfO2 Capacitors', ACS Appl. Mater. Interfaces, Aug. 2019
J31	M. Coll et al., 'Towards Oxide Electronics : a Roadmap', Applied Surface Science, vol. 482, pp. 1–93, 2019.
J32	R. Hentschel et al., 'Extraction of the active acceptor concentration in (pseudo-) vertical GaN MOSFETs using the body-bias effect', Microelectronics Journal, vol. 91, pp. 42–45, Sep. 2019
J33	M. Herzig, M. Weiher, A. Ascoli, R. Tetzlaff, T. Mikolajick, and S. Slesazeck, 'Improvement of NbOx-based threshold switching devices by implementing multilayer stacks', Semicond. Sci. Technol., 2019
J34	M. Herzig, M. Weiher, A. Ascoli, R. Tetzlaff, T. Mikolajick, and S. Slesazeck, 'Multiple slopes in the negative differential resistance region of NbOx-based threshold switches', J. Phys. D: Appl. Phys., 2019
J35	D. Hiller, P. M. Jordan, K. Ding, M. Pomaska, T. Mikolajick, and D. König, 'Deactivation of silicon surface states by Al-induced acceptor states from Al–O monolayers in SiO2', Journal of Applied Physics, vol. 125, no. 1, p. 015301, Jan. 2019
J36	M. Hoffmann et al., 'Unveiling the double-well energy landscape in a ferroelectric layer', Nature, vol. 565, no. 7740, p. 464, Jan. 2019
J37	M. Hoffmann, F. P. G. Fengler, B. Max, U. Schroeder, S. Slesazeck, and T. Mikolajick, 'Negative Capacitance for Electrostatic Supercapacitors', Advanced Energy Materials, vol. 9, no. 40, p. 1901154, 2019
J38	D. R. Islamov et al., 'Identification of the nature of traps involved in the field cycling of Hf0.5Zr0.5O2-based ferroelectric thin films', Acta Materialia, vol. 166, pp. 47–55, Mar. 2019
J39	M. B. Khan et al., 'Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires', Applied Sciences, vol. 9, no. 17, Art. no. 17, Jan. 2019
J40	A. Krause et al., 'In Situ Raman Spectroscopy on Silicon Nanowire Anodes Integrated in Lithium Ion Batteries', J. Electrochem. Soc., vol. 166, no. 3, pp. A5378–A5385, Jan. 2019
J41	B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, 'Direct Correlation of Ferroelectric Properties and Memory Characteristics in Ferroelectric Tunnel Junctions', IEEE Journal of the Electron Devices Society, pp. 1–1, 2019
J42	F. Mehmood et al., 'Bulk Depolarization Fields as a Major Contributor to the Ferroelectric Reliability Performance in Lanthanum Doped Hf0.5Zr0.5O2 Capacitors', Advanced Materials Interfaces, vol. 0, no. 0, p. 1901180, 2019
J43	T. Mittmann et al., 'Origin of Ferroelectric Phase in Undoped HfO2 Films Deposited by Sputtering', Advanced Materials Interfaces, vol. 6, no. 11, p. 1900042, 2019
J44	H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, 'Ferroelectric FETs With 20-nm-Thick HfO2 Layer for Large Memory Window and High Performance', IEEE Transactions on Electron Devices, vol. 66, no. 9, pp. 3828–3833, Sep. 2019
J45	H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, 'Recovery of Cycling Endurance Failure in Ferroelectric FETs by Self-Heating', IEEE Electron Device Letters, vol. 40, no. 2, pp. 216–219, Feb. 2019
J46	M. Neuber, O. Storbeck, M. Langner, K. Stahrenberg, and T. Mikolajick, 'Multi-staged deposition of trench-gate oxides for power MOSFETs', Journal of Vacuum Science & Technology B, vol. 37, no. 3, p. 032202, May 2019
J47	M. H. Park, Y. H. Lee, T. Mikolajick, U. Schroeder, and C. S. Hwang, 'Thermodynamic and Kinetic Origins of Ferroelectricity in Fluorite Structure Oxides', Advanced Electronic Materials, vol. 5, no. 3, p. 1800522, 2019
J48	M. H. Park, T. Mikolajick, U. Schroeder, and C. S. Hwang, 'Broad Phase Transition of Fluorite-Structured Ferroelectrics for Large Electrocaloric Effect', physica status solidi (RRL) – Rapid Research Letters, vol. 0, no. 0, p. 1900177, 2019
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J53	T. Schenk et al., 'On the Origin of the Large Remanent Polarization in La:HfO2', Advanced Electronic Materials, vol. 5, no. 12, p. 1900303, 2019
J54	S. Schmult, V. V. Solovyev, S. Wirth, A. Großer, T. Mikolajick, and I. V. Kukushkin, 'Magneto-optical confirmation of Landau level splitting in a GaN/AlGaN 2DEG grown on bulk GaN', Journal of Vacuum Science & Technology B, vol. 37, no. 2, p. 021210, Mar. 2019
J55	U. Schroeder, M. Materano, T. Mittmann, P. D. Lomenzo, T. Mikolajick, and A. Toriumi, 'Recent progress for obtaining the ferroelectric phase in hafnium oxide based films: impact of oxygen and zirconium', Jpn. J. Appl. Phys., vol. 58, no. SL, p. SL0801, Oct. 2019
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J58	F. Zimmermann et al., 'Green coloring of GaN single crystals introduced by Cr impurity', Journal of Luminescence, vol. 207, pp. 507–511, Mar. 2019

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C1	A. Aziz et al., 'Computing with ferroelectric FETs: Devices, models, systems, and applications', in 2018 Design, Automation Test in Europe Conference Exhibition (DATE), Mar. 2018, pp. 1289–1298
C2	T. Baldauf et al., 'Scaling Aspects of Nanowire Schottky Junction based Reconfigurable Field Effect Transistors. ' 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS). IEEE, 2019
C3	E. T. Breyer, H. Mulaosmanovic, S. Slesazeck, T. Mikolajick, and T. Mikolajick, 'Demonstration of versatile nonvolatile logic gates in 28nm HKMG FeFET technology', in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 2018, pp. 1–5
C4	M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, 'Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric Hf0.5Zr0.5O2', in 2018 IEEE International Electron Devices Meeting (IEDM), Dec. 2018, pp. 31.6.1-31.6.4
C5	M. Hoffmann, S. Slesazeck, and T. Mikolajick, 'Domain Formation in Ferroelectric Negative Capacitance Devices', in 2018 76th Device Research Conference (DRC), Jun. 2018, pp. 1–2
C6	B. Max, M. Hoffmann, S. Slesazeck, and T. Mikolajick, 'Ferroelectric Tunnel Junctions based on Ferroelectric-Dielectric Hf0.5Zr0.5.O2/ A1203Capacitor Stacks', in 2018 48th European Solid-State Device Research Conference (ESSDERC), Sep. 2018, pp. 142–145
C7	T. Mikolajick, U. Schroeder, and S. Slesazeck, 'Hafnium oxide based ferroelectric devices for memories and beyond', in 2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Apr. 2018, pp. 1–2
C8	I. O'Connor et al., 'Prospects for energy-efficient edge computing with integrated HfO2-based ferroelectric devices', in 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Oct. 2018, pp. 180–183
C9	M. Pesic, A. Padovani, S. Slcsazeck, T. Mikolajick, and L. Larcher, 'Deconvoluting charge trapping and nucleation interplay in FeFETs: Kinetics and Reliability', in 2018 IEEE International Electron Devices Meeting (IEDM), Dec. 2018, pp. 25.1.1-25.1.4
C10	S. Rai et al., 'A physical synthesis flow for early technology evaluation of silicon nanowire based reconfigurable FETs', in 2018 Design, Automation Test in Europe Conference Exhibition (DATE), Mar. 2018, pp. 605–608
C11	V. Sessi, H. Mulaosmanovic, R. Hentschel, S. Pregl, T. Mikolajick, and W. M. Weber, 'Junction Tuning by Ferroelectric Switching in Silicon Nanowire Schottky-Barrier Field Effect Transistors', in 2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO), Jul. 2018, pp. 1–4
C12	M. Simon et al., 'A wired-AND transistor: Polarity controllable FET with multiple inputs', in 2018 76th Device Research Conference (DRC), Jun. 2018, pp. 1–2
C13	S. Slesazeck, U. Schroeder, and T. Mikolajick, 'Embedding hafnium oxide based FeFETs in the memory landscape', in 2018 International Conference on IC Design Technology (ICICDT), Jun. 2018, pp. 121–124
C14	D. Tröger, M. Grube, M. Knaut, J. Reif, J. W. Bartha, and T. Mikolajick, 'Towards Full-area Passivating Contacts for Silicon Surfaces based on Al203-TiOxDouble Layers', in 2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC), Jun. 2018, pp. 2176–2179

Conference Proceedings 2018-2019

C15	J. Trommer et al., 'Off-state Impact on FDSOI Ring Oscillator Degradation under High Voltage Stress', in 2018 International Integrated Reliability Workshop (IIRW), Oct. 2018, pp. 1–5
C16	D. Bimberg, T. Mikolajick, and X. Wallart, 'Novel Quantum Dot Based Memories with Many Days of Storage Time : Last Steps towards the Holy Grail?', in 2019 19th Non-Volatile Memory Technology Symposium (NVMTS), Oct. 2019, pp. 1–4
C17	D. Tröger, M. Grube, M. Knaut, J. Reif, J. W. Bartha, and T. Mikolajick, "Passivating Contacts for Silicon Solar Cells made of Al2O3 and TiOx Nanolayer Systems," presented at the EU-PVSEC2018, 2018, p. 5
C18	E. T. Breyer et al., 'Ultra-dense co-integration of FeFETs and CMOS logic enabling very-fine grained Logic-in-Memory', in ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), Sep. 2019, pp. 118–121
C19	T. Chohan et al., 'Impact of BTI Stress on RF Small Signal Parameters of FDSOI MOSFETs', in 2019 IEEE International Integrated Reliability Workshop (IIRW), Oct. 2019, pp. 1–4
C20	M. Hoffmann, S. Slesazeck, and T. Mikolajick, 'Dynamic modeling of hysteresis-free negative capacitance in ferroelectric/dielectric stacks under fast pulsed voltage operation', in 2019 Device Research Conference (DRC), Jun. 2019, pp. 97–98
C21	P. D. Lomenzo et al., 'Ferroelectric Hf1-xZrxO2 memories: device reliability and depolarization fields', in 2019 19th Non-Volatile Memory Technology Symposium (NVMTS), Oct. 2019, pp. 1–8
C22	B. Max, T. Mikolajick, M. Hoffmann, S. Slesazeck, and T. Mikolajick, 'Retention Characteristics of Hf0.5Zr0.5O2-Based Ferroelectric Tunnel Junctions', in 2019 IEEE 11th International Memory Workshop (IMW), May 2019, pp. 1–4
C23	T. Mikolajick et al., 'Variants of Ferroelectric Hafnium Oxide based Nonvolatile Memories', in 2019 Device Research Conference (DRC), Jun. 2019, pp. 207–208
C24	T. Mikolajick et al., 'Next Generation Ferroelectric Memories enabled by Hafnium Oxide', in 2019 IEEE International Electron Devices Meeting (IEDM), Dec. 2019, pp. 15.5.1-15.5.4
C25	T. Mikolajick et al., 'Reconfigurable nanowire field effect transistors with volatile and nonvolatile configuration modes', Jun. 2019.
C26	T. Mikolajick, M. Herzig, M. Weiher, A. Ascoli, R. Tetzlaff, and S. Slesazeck, 'Threshold Switching and Analogue Switching in Niobium Oxide based Resistive Switches', Jul. 2019.
C27	T. Mikolajick et al., 'Basics and Device Applications of Ferroelectricity in Hafnium Oxide', Aug. 2019.
C28	T. Ravsher, H. Mulaosmanovic, E. T. Breyer, V. Havel, T. Mikolajick, and S. Slesazeck, 'Adoption of 2T2C ferroelectric memory cells for logic operation', in 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Nov. 2019, pp. 791–794
C29	U. Schroeder, T. Mikolajick, M. Hoffmann, B. Max, and S. Slesazeck, 'Negative Capacitance in Ferroelectric Hafnium Oxide', Apr. 2019.
C30	S. Slesazeck et al., 'Uniting The Trinity of Ferroelectric HfO2 Memory Devices in a Single Memory Cell', in 2019 IEEE 11th International Memory Workshop (IMW), May 2019, pp. 1–4
C31	S. Slesazeck, T. Ravsher, V. Havel, E. T. Breyer, H. Mulaosmanovic, and T. Mikolajick, 'A 2TnC ferroelectric memory gain cell suitable for compute-in-memory and neuromorphic application', in 2019 IEEE International Electron Devices Meeting (IEDM), Dec. 2019, pp. 38.6.1-38.6.4
C32	B. Suresh et al., 'Simulation of integrate-and-fire neuron circuits using HfO2-based ferroelectric field effect transistors', in 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Nov. 2019, pp. 229–232
C33	A. Toriumi et al., 'Material perspectives of HfO2-based ferroelectric films for device applications', in 2019 IEEE International Electron Devices Meeting (IEDM), Dec. 2019, pp. 15.1.1-15.1.4
C34	J. Trommer, M. Simon, S. Slesazeck, W. M. Weber, and T. Mikolajick, 'Eliminating Charge Sharing in Clocked Logic Gates on the Device Level Employing Transistors with Multiple Independent Inputs', in ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), Sep. 2019, pp. 134–137
C35	F. Winkler, M. Pešić, C. Richter, M. Hoffmann, T. Mikolajick, and J. W. Bartha, 'Demonstration and Endurance Improvement of p-channel Hafnia-based Ferroelectric Field Effect Transistors', in 2019 Device Research Conference (DRC), Jun. 2019, pp. 51–52

Monographs (Book Chapters) 2018-2019

M1	N. Balke, T. Schenk, I. Stolichnov and A. Gruverman, 'Chapter 7.1 - Piezoresponse Force Microscopy (PFM), in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 291 ff.
M2	E. T. Breyer and S. Slesazeck, 'Chapter 10.6 - Ferroelectric Devices for Logic in Memory, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 495 ff.
M3	F. Fengler, M. H. Park, T. Schenk, M. Pešic and U. Schroeder, 'Chapter 9.2 - Field Cycling Behavior of Ferroelectric HfO2-Based Capacitors, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 381 ff.
M4	M. Hoffmann, S. Slesazeck, T. Mikolajick, and C. S. Hwang, 'Chapter 10.5 - Negative Capacitance in HfO2- and ZrO2-Based Ferroelectrics', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, pp. 473–493.
M5	C. S. Hwang and T. Mikolajick, '11 - Ferroelectric memories', in Advances in Non-Volatile Memory and Storage Technology (Second Edition), B. Magyari-Köpe and Y. Nishi, Eds. Woodhead Publishing, 2019, pp. 393–441.
M6	J. Mueller, S. Slesazeck, and T. Mikolajick, 'Chapter 10.4 - Ferroelectric Field Effect Transistor', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, pp. 451–471.
M7	H. Mulaosmanovic and S. Slesazeck, 'Chapter 9.1 - Polarization Switching in HfO2-Based Devices, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 365 ff.
M8	H. Mulaosmanovic and S. Slesazeck, 'Chapter 10.7 - Ferroelectric Field Effect Transistor for Neuromorphic Applications, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 515 ff.
M9	M. H. Park, M. Hoffmann and C. S. Hwang, 'Chapter 5.2 - Pyroelectric and Electrocaloric Effects and Their Applications, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 217 ff.
M10	M. H. Park, T. Schenk, C. S. Hwang and U. Schroeder, 'Chapter 8 - Impact of Electrodes on the Ferroelectric Properties, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 341 ff.
M11	M. H. Park, T. Schenk, S. Starschich, C. M. Fancher, H. J. Kim, U. Bottger, C. S. Hwang, A. Toriumi, Xuan Tian and Uwe Schroeder, 'Chapter 3.5 - Effect of Surface/Interface Energy and Stress on the Ferroelectric Properties', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 145 ff.
M12	M. H. Park, T. Schenk and U. Schroeder, ,Chapter 3.1 - Dopants in Atomic Layer Deposited HfO2 Thin Films', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 49 ff.
M13	M. H. Park and U. Schroeder, 'Chapter 3 - Root Causes for Ferroelectricity in Doped HfO2', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 47 ff.
M14	M. H. Park, T. Shimizu, H. Funakubo and U. Schroeder, 'Chapter 5.1 - Structural Origin of Temperature-Dependent Ferroelectricity', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 193 ff.
M15	M. Pešic and L. Larcher, 'Chapter 9.3 - Modeling of Field Cycling Behavior of Ferroelectric Hafnia-Based Capacitors', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p.399 ff.
M16	M. Pešic and U. Schroeder, 'Chapter 10.2 - Antiferroelectric One Transistor/One Capacitor Memory Cell, in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, p. 425 ff.
M17	M. Pešić, U. Schroeder, and T. Mikolajick, 'Chapter 10.1 - Ferroelectric One Transistor/One Capacitor Memory Cell', in Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices, U. Schroeder, C. S. Hwang, and H. Funakubo, Eds. Woodhead Publishing, 2019, pp. 413–424.
M18	U. Schroeder, C. S. Hwang, and H. Funakubo, Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices. Elsevier Science, 2019.
M19	W. Weber, J. Trommer, A. Heinzig, and T. Mikolajick, 'Germanium-based polarity-controllable transistors', 2019, p. https://digital-library.theiet.org/content/books/10.1049/pbcs039e_ch2.

Invited Talks 2018-2019

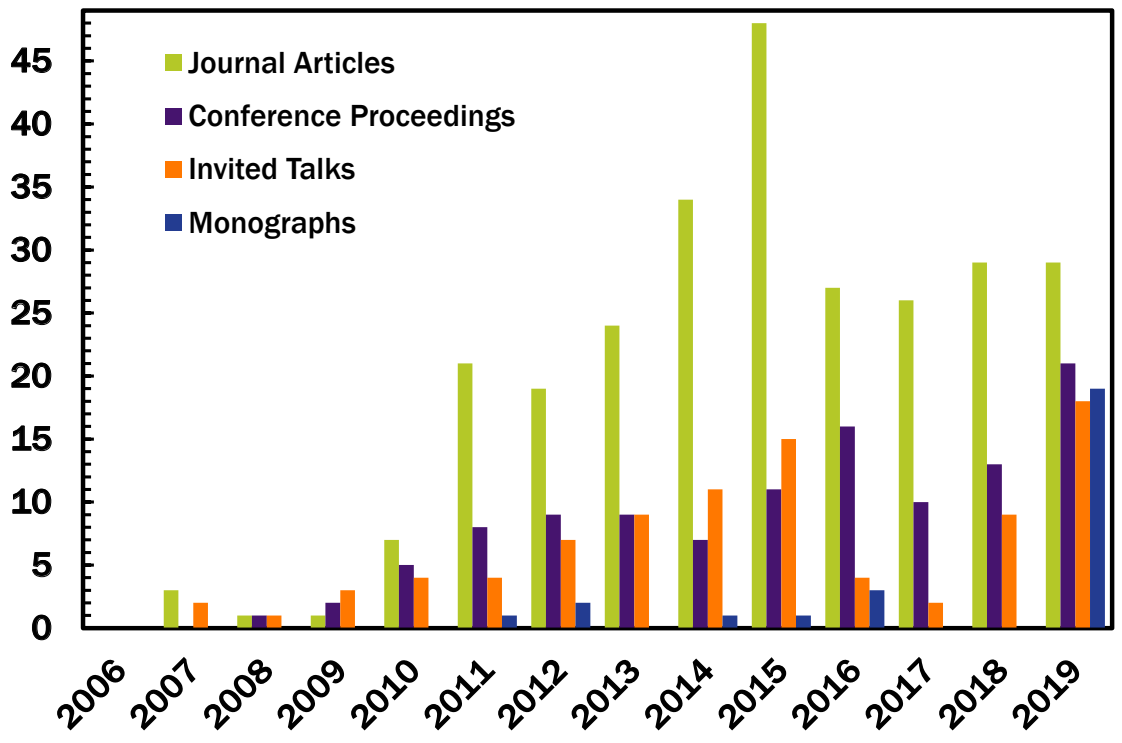
I1	T. Mikolajick, 'Next Generation Ferroelectric Memories enabled by Hafnium Oxide', presented at the International Electron Device Meeting (IEDM), San Francisco, USA, 2018.
I2	T. Mikolajick, B. Max, M. H. Park, M. Pešić, S. Slesazeck, and U. Schroeder, 'Capacitor and Tunnel Junction Based Memories Utilizing Ferroelectricity and Antiferroelectricity in Hafnium Oxide', presented at the NVMTS 2018, Sendai, Japan.
I3	T. Mikolajick et al., 'NVM Technologies Based on Ferroelectric Hafnium Oxide', presented at the CIMTECH, Perigia, 2018.
I4	M. H. Park, T. Schenk, T. Mikolajick, and U. Schroeder, 'Ferroelectricity in hafnia based thin films', presented at the CCMR, Incheon, Seoul, 2018.
I5	C. Richter et al., 'Robust ferroelectric performance by lanthanum doping in hafnium oxide', presented at the ISAF, Hiroshima, 2018.
I6	U. Schroeder, 'From FRAM to FeFET: Ferroelectric HfO2 based devices and their reliability', presented at the WODIM, Berlin, Germany, 2018.
I7	S. Slesazeck, 'Embedding hafnium oxide based FeFETs in the memory landscape', presented at the ICICDT, Otranto, Italy, 2018.
I8	S. Slesazeck, 'Hafnium oxide based ferroelectric devices for memories and beyond', presented at the VLSI-TSA, Hsinchu, Taiwan, 2018.
I9	P. D. Lomenzo, 'Unleashing Ferroelectricity in Hafnium and Zirconium Oxides for Next Generation Ferroelectric Devices', presented at the EM NANO, Nagano, Japan, 2019.
I10	P. D. Lomenzo, S. Slesazeck, T. Mikolajick, and U. Schroeder, 'Ferroelectric Hf1-xZrxO2 Memories: Device Reliability and Depolarization Fields', presented at the NVMTS, Durham, North Carolina, USA, 2019.
I11	T. Mikolajick et al., 'Basics and Device Applications of Ferroelectricity in Hafnium Oxide', presented at the 7th International Symposium on Integrated Functionalities (ISIF), Dublin, Ireland, 14.08 2019.
I12	T. Mikolajick et al., 'Variants of Ferroelectric Hafnium Oxide based Nonvolatile Memories', presented at the Device Research Conference, 28.06 2019.
I13	T. Mikolajick, U. Schroeder, M. Hoffmann, B. Max, and S. Slesazeck, 'Negative Capacitance in Ferroelectric Hafnium Oxide', presented at the MRS, Phoenix, USA, 26.04 2019.
I14	T. Mikolajick, 'Die Herausforderung künstliche Intelligenz - Bauelementeanforderungen und mögliche Lösungswege', presented at the Science Meets Industry, Chemnitz, Germany, Jan. 23, 2019.
I15	T. Mikolajick, 'Impact of Process Parameters on the ferroelectric properties of doped hafnia films', presented at the EMRS spring meeting 2019, Nice, France, 31.05 2019.
I16	T. Mikolajick, 'Reconfigurable nanowire field effect transistors with volatile and nonvolatile configuration modes', presented at the EMRS spring meeting 2019, Nice, France, 31.05 2019.
I17	T. Mikolajick, 'Threshold Switching and Analogue Switching in Niobium Oxide based Resistive Switches', presented at the Memrisys 2019, Dresden, Germany, 11.07 2019.
I18	H. Mulaosmanovic, 'Ferroelectric hafnium oxide: an emerging material for data storage and beyond', presented at the JSPS165 International Symposium, Nagoya, Japan, 2019.
I19	H. Mulaosmanovic, 'Ferroelectric HfO2 for Memory Applications and Unconventional Computing', presented at the SSDM, Japan, 2019.
I20	U. Schroeder, 'Ferroelectric Hafnium and Zirconium Oxide: Novel Devices and Applications', presented at the FMA, Japan, 2019.
I21	U. Schroeder, 'Ferroelectric Hafnium Oxide and its applications in non-volatile memories, negative capacitance elements, and neuromorphic networks', presented at the ISAF, Lausanne, Switzerland, 2019.
I22	U. Schroeder, 'Ferroelectric HfO2 for Memory Applications and Unconventional Computing', presented at the SSDM, Japan, 2019.
I23	U. Schroeder, 'Root causes for ferroelectricity in dioped HfO2', presented at the EMA, Orlando, 2019.
I24	S. Slesazeck, 'Switching kinetics in Hafnium oxide based ferroelectric / dielectric bilayer stacks', presented at the INFOS, Cambridge, UK, 2019.
I25	S. Slesazeck, 'The Trinity of Ferroelectric Memory Devices for Neuromorphic Computing', presented at the EMRS, Warsaw, Poland, 2019.
I26	I. Stolichnov, M. Cavalieri, T. Mittmann, U. Schroeder, and A. M. Ionescu, 'HfO2-based ferroelectrics: polarization dynamics at the nanoscale in the application-relevant geometries', presented at the ISAF, Lausanne, Switzerland, 2019.

Education

PhD thesis

T1	J. Beister 'Untersuchung des elektronischen Transports an 28nm MOSFETs und an Schottky-Barrieren FETs aus Silizium-Nanodrähten', TU Dresden, Dresden, 2018.
T2	P. Hofmann 'Hybride vapour phase epitaxy growth, crystal properties and dopant incorporation in gallium nitride', TU Dresden, Dresden, 2018.
T3	F. P. G. Fengler 'Analysis of the field cycling behavior of ferroelectric capacitor structures based on hafnia zirconia films', TU Dresden, Dresden, 2019.
T4	S. Knebel 'Ultra dünne hoch Epsilon Oxide zur Verwendung in modernen CMOS Anwendungen unter dynamischen Stressbedingungen', TU Dresden, Dresden, 2019.

Publication Statistics



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