Energy Efficient Embedded Non-Volatile Memory & Logic Based on Ferroelectric $Hf(Zr)O_2$

3εFERRO focuses on competitive, scalable FeRAM and logic-in-memory based on Si-compatible, ferroelectric $Hf_xZr_{1-x}O_2$. We report interface engineering, capacitor integration, FeFET and FeRAM logic design.

Energy efficiency

The 3εFERRO consortium researches energy efficient non-volatile memory and logic devices based on Si-compatible ferroelectric $HfZrO_2$ (HZO) to provide advanced embedded solutions for normally-off microcontroller units used in IoT. The consortium is a balanced mix of large technology development laboratories and academia in partnership with ST Microelectronics to address the complex issues associated with materials optimization, circuit design, device fabrication and integration.

At A Glance

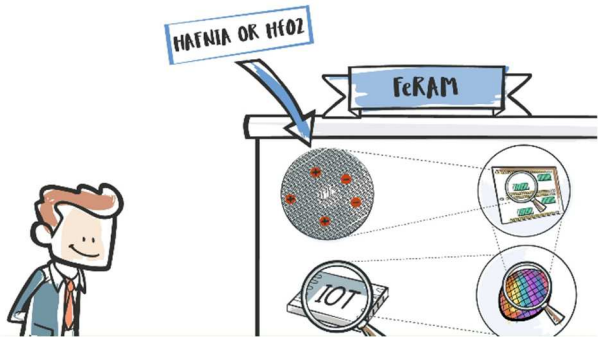
Coordinator : nick.barrett@cea.fr
Website : https://www.3eferro.eu.
Duration: 01/01/2018 – 30/06/2021

Funding scheme: RIA
EC Contribution: € **3.99**m

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 780302

3εFERRO Video now available

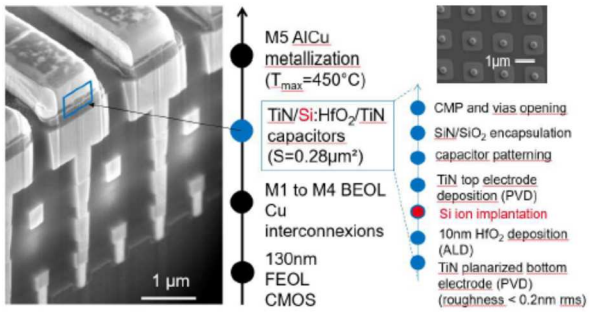
The 3εFERRO partners realized a video presentation of the project to a wide audience, available here:



https://www.youtube.com/watch?v=M8tL-nN7G-A

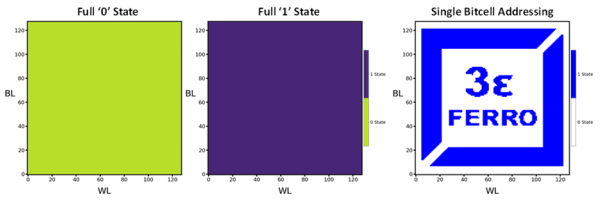
Reliability: zero bitfail in 16 kbit 1T-1C FeRAM arrays

Following the 16 kbit 1T-1C FeRAM new design, demonstrator #2 CMOS wafers with optimized sense amplifiers have been processed at CEA-LETI. 1T-1C FeRAM distributions were measured.



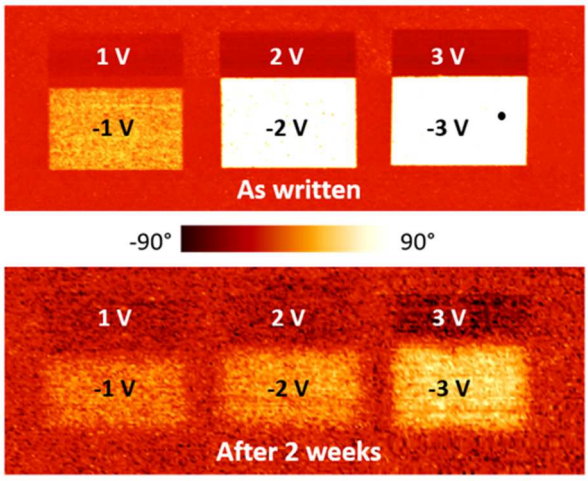
10 nm Si-implanted HfO_2 is demonstrated to be ferroelectric for the first time when integrated in a Back-End-Of -Line (BEOL) 130 nm CMOS. Scaled 0.28µm² capacitors demonstrate excellent endurance (10^9 cycles measured at 4V, extrapolated to be 10^{12} at 3V), with tight coercive field distributions at wafer scale and excellent data retention at 85°C.

Zero bitfail has been recorded in the 16kbit 1T-1C array of the 600 nm. The Full '0' and Full '1' states are read after write operations adopting pulses of 2 µs width at 4.8 V. The test vehicle allows to address and read the individual bitcells. Patterns like the 3εFERRO logo can thus be stored in the array.



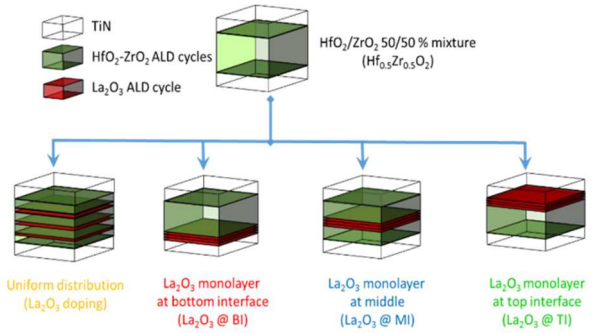
Charge injection in $HfZrO_2$

There is a wide range of coercive fields quoted in the literature for HfO_2 or $HfZrO_2$ thin films. One reason may be the competing effects of applied bias and potential barrier set up by charge injection and trapping at defect sites. We have investigated this using piezo-response force microscopy and low energy electron microscopy to quantify the relative contributions of charge and domain switching to observations. Charge injection plays an important role in device reliability.



AlO and LaO electrical optimization of $HfZrO_2$ films

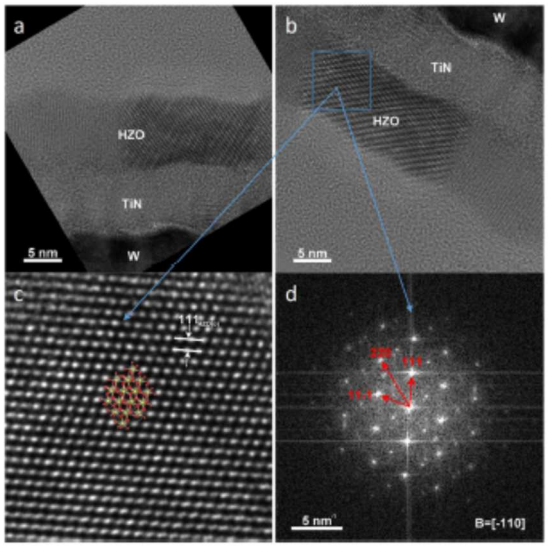
Comparing both LaO_x and AlO_x interlayers, both showed improved leakage and cycling endurance, but AlO_x decreased remanent polarization and degraded wake-up behaviour. This indicates that the best condition is still a 0.5 nm LaO_x at the bottom TiN electrode. In addition, retention tests were performed on HZO based capacitors with AlO_x or LaO_x interface at elevated temperatures of 75°C.



A LaO_x monolayer (about 0.5 nm LaO_x) showed the highest pristine remanent polarization values and low wake-up effects compared to the uniformly mixed case. Looking at the best position of the LaO_x monolayer, the interface between the bottom TiN electrode and $HfZrO_4$ indicated lower fatigue. This result can be nicely seen as a clear cycling improvement with almost no wake-up effect in relation to the undoped and mixed doped case.

$HfZrO_2$/electrode interface structure

Structural investigations were performed on samples with different electrodes, as well as on samples with different layers introduced at the interface between the HZO layer and TiN electrodes (e.g. Al_2O_3, Ti, etc.). The presence of the ferroelectric orthorhombic phase of HZO was evidenced in all samples, although the amount of this phase appears to vary depending on the deposition process of HZO and composition of the metal-ferroelectric-metal stack in terms of materials used for electrodes and interface layers.

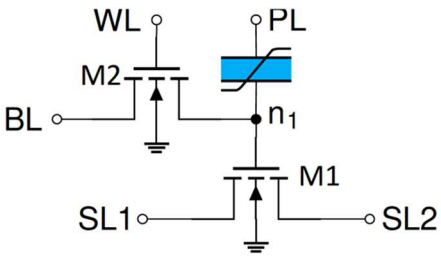


As an example, very good results were obtained for sample with the composition Al_2O_3/HZO/TiN/W/Si, in which the orthorhombic phase appears to be dominant, as revealed by TEM analysis.

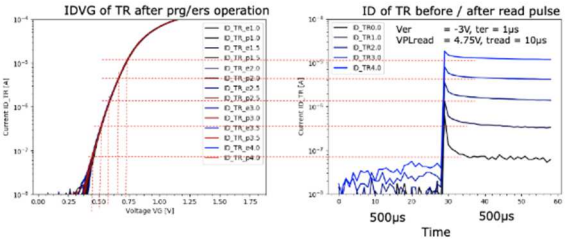
2T-1C memory cell shows multi-level possibilities

The 2T-1C memory cell structure is a good fit for exploring design possibilities offered by a given fabrication technology, as it allows multiple operating modes for a single device: FeFET-like operation, FTJ-based operation mode, and a DRAM-like operation mode; these being different ways of reading a value written into the ferroelectric capacitor. It also sidesteps usual difficulties that can be had when programming a ferroelectric capacitor in some devices like the FeFET, by providing a direct access to both poles of the capacitor. While a FeFET version had already been fabricated, the use of a BEoL ferroelectric capacitor is a more natural approach and enables greater design flexibility as well as improved overall performance.

The figure depicts the circuit schematic of the 2T-1C cell that was designed and characterized in a collaborative work between ECL-INL and NaMLab. A select transistor M2 connects the ferroelectric capacitor to the BL and is controlled via the WL.



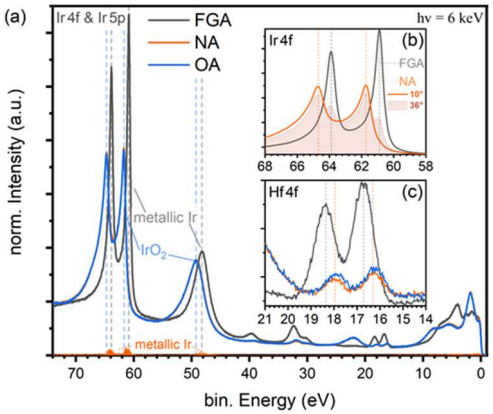
A second transistor M3 is the read transistor that is used to monitor the potential of floating node n1 during read operation by measuring its S/D current via SL1. Finally, the PL connects to the second terminal of the ferroelectric capacitor.



The second Fig. shows the measurement results on a 300nm diameter ferroelectric capacitor for different programming (ID_TR_p*) and erase (ID_TR_e*) voltages [1V..4 V], and a 10µs, 4.75V read pulse. On the left-hand side, the I_D-V_G characteristic of M3 is shown as characterized beforehand by sweeping M3's gate voltage V_G via the BL while switching on the access transistor M2. On the right-hand side, the measured S/D current over time within 500 µs before and 500 µs after applying the PL pulse is plotted. From this, current levels together with the I_D-V_G characteristic of M3 enable the internal node voltage of n1 to be determined, as illustrated by the red dashed lines. It can be clearly seen that multiple current levels can be differentiated, which correspond to different programming voltages (V_{pr} = [0, 1, 2, 3 and 4 V]). Hence, besides proper functionality of the cell, multi-level storage can also be demonstrated. This can be of great interest either to increase the effective storage density of the 2T-1C technology, or to implement quasi-analog approaches for example in neuromorphic architectures.

IrO_2 electrode engineering

Iridium oxide electrodes (IrO_2) have been proven to act as an oxygen supplier in ferroelectric MFM structures. HAXPES analysis has been carried out by FZJ on IrO_2/HZO/IrO_2 samples, prepared by using different atmospheres for the crystallization anneal process: oxygen (OA), nitrogen (NA) or in forming gas (FGA) (90% nitrogen, 10% hydrogen).



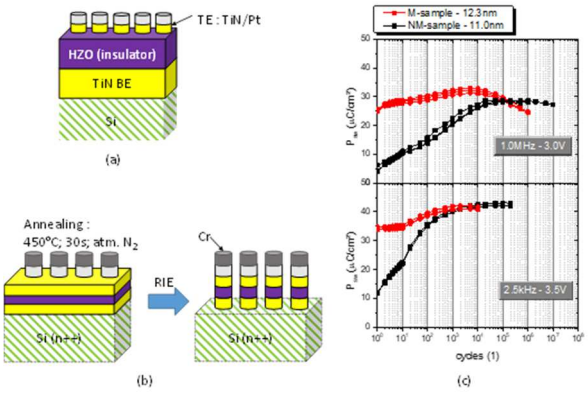
The IrO_2 electrode remains chemically stable for annealing in oxygen atmosphere. For annealing in nitrogen atmosphere, a chemical reduction of the IrO_2 electrode starts and results in metallic Ir layer on top of the IrO_2 electrode. Finally, forming gas annealing causes a complete reduction of the IrO_2 top electrode into metallic Ir.

Performance of $HfZrO_2$ mesas made by sputtering

The most widely used growth technique for ferroelectric hafnia is atomic layer deposition. Sputtering could offer a rapid, flexible and low cost alternative. Two different TiN/HZO/TiN 1C structures deposited by magnetron sputtering on silicon were fabricated. The maximum remanent polarization is higher than 21 µC/cm² for both samples, but a strong difference is observed in the electrical behaviour.

For the mesa sample (M-sample), the difference between the maximum and initial remanent

polarization is only 3 µC/cm², whereas it is around 14 µC/cm² in the non-mesa case (NM-sample).



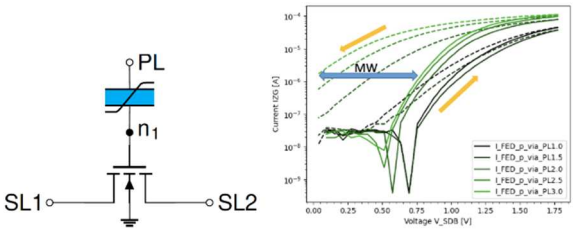
The two different structures realized have performances among the best in sputtering, but their behaviours are completely different. Mainly, the mesa structure presents a significantly reduced wake-up effect but a lower endurance. The wake-up effect is one of the major issues for ferroelectric HfO_2-based memory devices.

Leakage mechanisms

Current-voltage (I-V) characteristics recorded at different temperatures have shown a weak dependence of the current magnitude on temperature. Classic conduction mechanisms reported for perovskite ferroelectrics do not well describe the observed temperature and voltage dependence of the leakage current in HZO capacitors with top and bottom TiN contacts. Possible candidates of conduction mechanism, that satisfactory fit the experimental data for the leakage current are: phonon assisted tunneling between traps or Fowler-Nordheim tunneling with weak dependence on temperature of the potential barrier at electrode interfaces.

First experimental results from pseudo-FeFET structure

Back-End-of-Line (BEoL) integration of ferroelectric capacitors (FeCaps or FeRAMs, as enabled by the MAD200v3 run at CEA-LETI) obviously precludes the availability of FeFET type structures which require the direct integration of a ferroelectric oxide in the gate stack of FETs. However, it is possible to replicate FeFET operation with this BEoL technology by connecting the ferroelectric capacitor device to the gate terminal of a FET, thus achieving a Metal-Ferroelectric-Metal-Oxide-Semiconductor stack, with the second metal layer replaced by a via from the metal 4 layer up to the ferroelectric layer. This is known as a pseudo-FeFET or FeFET generation 2. The structure has not been investigated previously, and can open up new design possibilities since endurance is improved through the use of BEoL devices, and further the physical area of the ferroelectric capacitance can be quite different from that of the transistor gate. Test structures were designed at ECL-INL and fabricated at CEA-LETI, using various capacitor sizes (from 300 nm to 500 nm) to compensate possible variability due to the fabrication, as well as simulation unknowns.



First measurement results carried out by NaMLab reveal basic functionality of the pseudo-FeFET. In these measurements, the I_D-V_G characteristic is depicted after application of a negative pulse to the PL with increasing amplitude which can be considered as an erase pulse, yielding the high-V_{th} state. During forward sweep (plotted as a solid line) the device is programmed and alters its threshold voltage to lower values, resulting in a virtually steeper sub-threshold slope. The resulting V_{th} state can be observed in the backward sweep (plotted with a dashed line). The memory window MW is defined as the difference between the threshold voltages of the erased and programmed states (blue arrow). With increasing PL-amplitude to erase the device, an increasing memory window of up to 0.8V is extracted.

Coda

The 3εFERRO project finished on June 30th 2021 and the project wrap up meeting takes place in Grenoble at the end of September 2021. This fifth newsletter summarizes some of the significant results from the last year of the project, but more will be forthcoming in journal publications and conference presentations currently being prepared or already submitted. The website provides the full publication list.

In the meantime we would like once again to acknowledge the Horizon 2020 funding, the support of our respective institutes and the enthusiasm and hard work of all from CEA, NaMLab, INL, NCSRD, FZJ, EPFL, NIMP and ST Microelectronics.